IN-PLANE CARBON NANOTUBE FIELD EMITTERS FOR HIGH TEMPERATURE INTEGRATED ELECTRONICS

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By

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DEDICATION

For my wife, Andréa, whose love and support has been there since the beginning
and is always there for me when I need it most.

For my parents, who have challenged me to be the very best I could be.

For my family and friends who have supported me along the way.

For my grandparents too soon departed,

Andrew M. Hunt
Harold P. Monica
Dr. and Mrs. Richard P. Sexton

You are loved and you are missed.
I hope I have made you proud.
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ABSTRACT

Lateral carbon nanotube (CNT)-based field emission devices have been developed for the purpose of fabricating diodes, triodes, and ultimately integrated circuits. The goal of this research is to create CNT-based field emission devices that offer high performance operation in harsh environments, particularly high temperature. Silicon based technologies suffer from an inherent inability to operate at temperatures above ~300°C; however, a need still exists for such electronics. The devices developed by this research seek to address the need for robust microelectronics capable of wide temperature range operation without the need for elaborate cooling systems.

The field emitter structures consist of carbon nanotubes that are created using one of two distinct techniques: dielectrophoretic assembly or thermal chemical vapor deposition synthesis. I will discuss how such techniques can be used to create lateral CNT structures suitable for planar field emission while also enabling complete compatibility with modern semiconductor processing techniques. The electrical and thermal performance results of planar CNT field emitters operating in diode and triode configurations are also reported.
Carbon nanotube based field emission devices, such as those I have developed, have characteristics that could result in benefits to an exceedingly wide range of applications beyond operation in harsh environments. High-frequency analog applications are particularly of interest because of the very low capacitances and the high current/unit area capability of typical CNT field emitters, which is in the Amps/cm² range. Also, since field emitted current is a very strong function of the applied electric field, these devices will undoubtedly find potential use in applications requiring large gain.
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FIGURE 65: Cross-section and top-down views of the substrate after the first lithographic step. Here, a small rectangular window is opened in the photoresist and Ti layers to expose the SiO₂ below. The photoresist and Ti layers will serve as an etch mask for an RIE process which will remove the majority of the SiO₂. A brief BOE etch will be performed to complete the removal of the SiO₂.

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FIGURE 78: Electrical setup used for the thermal testing of a device operating in a diode configuration. A resistive heater (not shown) is placed under the substrate to heat the device from room temperature to 200 °C. 153

FIGURE 79: I-E data plots for a device operating in a diode configuration for several different temperatures. The spread in the sweeps is likely due to gas desorption from the CNTs and should decrease with time. The device being tested was not
SUBJECTED TO ANY “BURN IN”, THUS THE SPREAD IN THE ELECTRIC FIELD VALUES IS TO BE EXPECTED.

**FIGURE 80:** FOWLER-NORDHEIM PLOTS AND THE CORRESPONDING LINEAR FIT FROM I-E DATA TAKEN AT A SERIES OF DIFFERENT TEMPERATURES. THE DEVICE BEING TESTED WAS OPERATED IN A DIODE CONFIGURATION UNDER HIGH VACUUM.

**FIGURE 81:** SCHEMATIC REPRESENTATION OF THE CURRENT DEVICE FABRICATED USING THERMAL CHEMICAL VAPOR DEPOSITION. (LEFT) TOP-DOWN VIEW SHOWING ANODE, CATHODE, GATES, AND CNTs. THE DASHED YELLOW RECTANGLES INDICATE ALTERNATE GATE LOCATIONS. (RIGHT) CROSS-SECTION OF DEVICE CONCEPT SHOWING THE ANODE, CATHODE, AND LATERALLY GROWN CNTs (GATES OMITTED FOR CLARITY).

**FIGURE 82:** I-V AND F-N PLOTS FOR A TYPICAL THIRD GENERATION THERMAL CVD BASED DEVICE TESTED IN A DIODE CONFIGURATION UNDER HIGH VACUUM (1×10⁻⁶ TORR).

**FIGURE 83:** ELECTRICAL SETUP USED FOR TESTING DEVICES IN A TRIODE CONFIGURATION.

**FIGURE 84:** GATE CURRENT AND ANODE VOLTAGE AS A FUNCTION OF GATE VOLTAGE FOR A DEVICE FIELD EMITTING A CONSTANT CURRENT OF 10 NA.

**FIGURE 85:** PLOT OF REGION 2 FROM FIGURE 84 SHOWING THE ANODE VOLTAGE AND GATE CURRENT AS A FUNCTION OF GATE VOLTAGE.
1 Introduction

Vacuum microelectronics (VME) is the science and technology of fabricating micron-scale devices whose operation relies on the transport of electrons through a vacuum. As a technology, vacuum microelectronics offers numerous advantages over semiconductor-based devices. Within a vacuum, electrons travel faster with no energy dissipation in contrast to a solid-state semiconductor structure where scattering is always present. This translates into more rapid modulation of the device and the potential for significantly higher electron energies. As a result, vacuum microelectronic devices can operate at higher frequencies and higher power compared to their semiconductor counterparts. In addition, VME devices can operate over a wide temperature range and in high radiation environments due to the inherent properties of field emission and electron transport through vacuum. Field emission as an electron emission mechanism is relatively temperature independent while a vacuum is unaffected by ionizing radiation. Conversely, semiconductor technology requires shielding from ionizing radiation (which may cause charging, physical damage, and increases in mobile charge carrier density) and thermal control to maintain stable operating characteristics. Table 1 gives a brief comparison of vacuum microelectronic devices with semiconductor technology.
Table 1: Properties of Solid State and VME Devices [1].

<table>
<thead>
<tr>
<th>Properties</th>
<th>Solid State Devices</th>
<th>VME Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current density</td>
<td>$10^4 - 10^5$ A/cm$^2$</td>
<td>$\sim 2 \times 10^3$ A/cm$^2$</td>
</tr>
<tr>
<td>Structure</td>
<td>Solid-solid interface</td>
<td>Solid-vacuum interface</td>
</tr>
<tr>
<td>Electron energy</td>
<td>$&lt; 0.3$ eV</td>
<td>Several to 1000 eV</td>
</tr>
<tr>
<td>Cutoff Frequency</td>
<td>$&lt; 20$ GHz (Si), $&lt; 100$ GHz (GaAs)</td>
<td>$&lt; 100$-500 GHz</td>
</tr>
<tr>
<td>Radiation hardness</td>
<td>Poor</td>
<td>Excellent</td>
</tr>
<tr>
<td>Temperature range</td>
<td>-30 to +50 °C</td>
<td>$&lt; 500$ °C</td>
</tr>
<tr>
<td>Fabrication</td>
<td>Well established</td>
<td>Not well established</td>
</tr>
</tbody>
</table>

Currently, vacuum microelectronics is an active area of research with many different potential applications [2-5]. In most instances, these devices rely upon a sharpened tip fabricated from a conductive material. Materials that have been used include semiconductors such as GaAs [6] and silicon [1], molybdenum [7], platinum [8], tungsten [9], diamond [10], and carbon nanotubes (CNTs) [2, 11-15]. The purpose of these sharp tips is twofold; to localize the electron emission site and to concentrate and enhance the local electric field, thus reducing the operating voltages. Typically these devices adopt a geometry similar to Spindt emitters with a conical metallic tip protruding through a micron-sized gated aperture, shown in Figure 1 [1, 16].

![Figure 1](image-url)
which the tip protrudes, and (3) a separate anode, typically a metallic surface
or phosphor screen.

For most practical applications such as displays and technologies requiring an
electron gun, the field-emitted electrons from a VME device are emitted
perpendicular to the substrate and collected on an anode separate from the emitting
substrate. Though this device structure is ideal for such applications, it does not lend
itself to large-scale integrated circuit (IC) fabrication because the anode is fabricated
separately from the rest of the device. To solve this issue, the emitted electrons
should be made to travel parallel to the substrate surface rather than perpendicularly
outwards and away from it. Achieving this lateral electron emission can be done by
simply rotating the emitters into the plane of the substrate (Figure 2). This new
device structure affords numerous advantages to the more conventional vertical
emission geometry. Perhaps the most significant advantage is that all device
electrodes (anode, cathode, and gate) are fabricated on the same substrate,
eliminating the need for separate anodes and anode-to-cathode alignment.
Furthermore, the electrodes are patterned by standard photolithography enabling
inter-electrode spacings on the order of a micron or less leading to devices that can
operate at less than 10 V. Lastly, a planar device geometry is compatible with wafer-
level processing techniques allowing for simplified integration into ICs and batch
fabrication. Despite the advantages lateral field emission offers, relatively few
attempts have been made to fabricate VME devices with such a planar geometry and
emission parallel to the chip surface since most early research has focused on display technologies relying on vertical emission [6, 17-20].

![Cross-sectional representation of (Left) vertical (and (Right) in-plane field emission geometries.](image)

The focus of this research is to develop a VME technology that utilizes carbon nanotubes as field emitters in a planar micro-triode geometry. The proposed CNT micro-triode is based on arrays of multiple, aligned carbon nanotube field emitters. Like their macroscopic vacuum electronic predecessors, these nanotube field emission triodes are immune to ionizing radiation. They also operate over an extremely wide temperature range (~20 K to ~900 K) with minimal changes in performance. Furthermore, the incorporation of methods for depositing or growing CNT emitters in a planar geometry permits parallel fabrication using microelectronic processing techniques. Each CNT array consists of hundreds to tens of thousands of nanotubes, thus every array has an inherent redundancy enabling longer lifetimes and more stable device performance. Using CNT arrays in a field-emission triode rather than single CNTs in a field-effect transistor [21-27] also bypasses the most serious obstacle to CNT electronics: it is irrelevant whether the CNTs are semiconducting or metallic. Additionally, the gate-source and gate-drain capacitances and the leakage
currents are small, allowing for high-speed operation and low power consumption, two critical aspects required of modern day electronics.
2 Historical Background

2.1 Foundations

Towards the end of the 19th Century, numerous scientists and inventors were conducting increasing amounts of research on various types of sealed and evacuated tubes. Geissler tubes, for demonstrating electrical discharge phenomena, and Crookes tubes, for exploring phosphorescent effects seen in Geissler tubes, are two prominent examples. Though these tubes were primarily for specialized scientific applications, the knowledge and insight gained from the investigations would lay the foundation for, and eventually lead to, the invention of the first vacuum triode.

Although thermionic emission was first discovered in 1873 by Guthrie in Britain, it took a rediscovery by Thomas Edison in 1880 before generating significant interest. At the time, Edison was developing light bulb systems and trying to determine the reason for bulb filament failure and uneven blackening of the glass envelope in his incandescent light bulbs, both of which resulted in undesirably short lifetimes. Though filament breakage was an issue, the limiting factor for Edison’s bulb was the gradual blackening of the glass envelope that would cause the bulb to dim over time, eventually rendering it useless. Initially, the blackening was attributed to carbon atoms ejected from the carbon filament. Despite an incomplete understanding of the phenomena, it was known at the time that particles leaving the electrode were negatively charged. As a result Edison designed numerous experiments to find a
means of preventing the particles from depositing on the glass surface. In one particular trial, a second electrical element was added to attract the ejected particles away from the glass envelope. While experimenting with the polarity of the additional element, Edison observed that with the second element biased positive with respect to the hot filament, a current would flow. Upon reversing the polarity on the second element, no current flowed. First dubbed the Edison effect lamp and known today as the thermionic diode, Edison would patent his invention in 1883, though he could not explain how it worked.

2.2 The Thermionic Vacuum Tube

In the years that followed the initial invention, Edison neglected his thermionic diode as he was developing his light bulb system. However, other scientists and engineers recognized the importance of Edison’s discovery and began researching it further. In 1890, J. A. Fleming’s paper was the first report of a thermionic diode as an electronic device when he observed signal rectification [28]. Seven years later in 1897, J. J. Thomson would reveal his apparatus to measure the charge-to-mass ratio of the electron [29]. Today this event is taken to officially mark the discovery of the electron. In his 1899 paper Thomson would go on to discover that the particles liberated in photoemission and thermionic emission were also electrons [30]. In 1904 Fleming would revisit his work with the Edison effect while at Marconi Wireless Telegraph Company in England. He believed that if the low frequency rectification he observed using an Edison effect diode in 1890 was possible, then rectification of
radio frequency (RF) signals may be as well. His subsequent experiments were successful and the kenotron was born [31]. This device would later be known as the Fleming valve and ultimately, the diode. These technological advancements finally culminated in 1906 when L. de Forest added a grid to the thermionic diode of Fleming, thus creating the audion, later known as the triode [32]. From his experiments, de Forest discovered the additional wire grid electrostatically controlled the current passing between the hot filament and the collection plate. As a result, the device was an excellent and very sensitive voltage amplifier. Nine years after de Forest constructed his audion, scientists at General Electric research laboratory led by Irving Langmuir developed the first true vacuum tube in 1915.

Since their invention up through the 1950s, vacuum tubes were widely used as essential components for radio, television, numerous industrial and military applications, and scientific instruments. However, this popularity would eventually end with the advent of semiconductor transistors, invented by Bardeen, Brattain, and Shockley in the 1950s [33]. By the 1960s, integrated circuits had been developed and many thought the time for employing vacuum tube technology had come to an end. While vacuum tubes would still offer performance advantages in specific high power applications such as microwave ovens, industrial RF heating, power amplification for broadcasting, and various military technologies, they had numerous disadvantages when compared to solid-state transistors. Perhaps the main disadvantage of the vacuum tube was the required heating of the tube filament to
temperatures exceeding 1000 °C for electron generation. This unavoidable inefficiency in thermionic devices, along with a relatively large size and fragility would lead to the downfall of vacuum tube technology. In comparison, semiconductor transistors could be fabricated more than a thousand times smaller, required no heating, and were more efficient. The net result was a sweeping replacement of most vacuum tubes with the smaller, cheaper, and more efficient solid-state transistors. However, the foundation had been laid for an eventual resurgence of vacuum devices beginning in the 1960s with the combination of two technologies leading to the development of vacuum microelectronics (VME).

### 2.3 Vacuum Microelectronics

Historically, the naissance of vacuum microelectronics hinged upon two important technological developments. The first was the extensive development of microfabrication technology for the semiconductor industry, particularly chip level large-scale integration of devices. Since the 1950s, manually machined and assembled vacuum tubes had already demonstrated operating frequencies up to 4 GHz [34, 35], so it would not seem difficult to envision a new microfabrication technique capable of producing miniaturized devices smaller than manually assembled tubes having significantly higher operating frequencies. The second technological development directly addressed the inefficiencies of electron generation inherent to thermionic-based devices. Field emission, a quantum mechanical tunneling phenomenon in which an electron escapes from a solid surface
into the surrounding vacuum, provided a more advantageous form of electron generation. Perhaps the primary benefit of field emission is that it does not require the heating of a filament. Instead, unheated “cold” cathodes under intense electric fields generate the necessary electrons. In addition, field emission also offers immediate response to electric field variations, resistance to temperature changes and radiation, and an exponential current-voltage relationship where a small change in voltage generates a large change in emission current. Though it possesses many advantages over thermionic emission, field emission does require very large electric fields, on the order 10 MV/cm, to extract electrons from the solid surface. To deal with this issue, metallic needles were wet etched to produce tip curvatures of a few hundred nanometers. The resulting high aspect ratio needles served to concentrate and enhance the local electric field at the tip apex, however, even the most advanced needles required thousands of volts to draw useful currents.

Extensive research during the 1950s – 1970s on field emission from sharpened needles led to the conclusion that the etched needles had numerous limitations when employed as cathodes in miniaturized devices. Such limitations included the necessity for high operating voltages (1000s of volts), high vacuum requirements (<10⁻⁹ torr), and limited cathode lifetimes due to sputtering from high energy ions created from electron impact ionization in the vacuum gap. Despite the limitations, field emission cathodes using etched needles found success in numerous devices
such as cathode ray tubes, electron microscopes, electron beam lithography, and microwave amplifiers.

As these revelations regarding field emission from sharpened needles were taking shape, K. R. Shoulders proposed a groundbreaking idea in 1961. In his article, he proposed a field emission device of micron size with switching times of $10^{-10}$ seconds that could (1) operate at 50 volts, (2) have high input impedance, (3) be insensitive to temperature effects to 1000 °C and to ionizing radiation, and (4) have lifetimes of hundreds of years [36]. Though ambitious, the device proposed by Shoulders was perfectly suited to utilize the microelectronic processing technologies developed by the semiconductor industry.

This idea was greeted with great enthusiasm, however, by the mid-1960s much of the interest had waned due to the aforementioned difficulties in using etched needles as electron emitters. Then, in 1968, C. A. Spindt of Stanford Research Institute (SRI), hired by Shoulders to carry on the work, succeeded in fabricating Shoulders’ proposed device [16]. The new field emitter structure, known as the Spindt emitter (Figure 1), comprised a multilayer structure consisting of a Mo gate, SiO$_2$ insulator, and Mo cathode cones, all fabricated using thin film vacuum deposition techniques. Operation of Spindt cathodes, referred to as field emitter arrays (FEAs), typically required a gate voltage of 100 volts and could realize device densities of $10^7$ emitters
per square centimeter. Device lifetimes often exceeded 10,000 hours and noise reduction could be achieved through statistical averaging over many emitters [37].

Due to their outstanding performance, devices built with FEAs immediately became attractive, especially for flat panel display technology and high frequency vacuum tube devices. In the years that followed, numerous improvements on the Spindt emitter were made, ultimately resulting in improved operation, longer lifetimes, and higher emission currents; however, beginning in the mid-1990s scientists began searching for novel, more robust emitter materials to incorporate into FEAs to deal with the lifetime and degradation issues. Coincidentally, a new and unique material perfectly suited for the task had just been discovered.

### 2.4 A Novel Cathode Material: Carbon Nanotubes

In 1991, while working for the NEC Fundamental Research Laboratory in Tsukuba, Japan, Sumio Iijima observed peculiar nanoscopic threads emanating from a sample of soot [38]. Comprised entirely from carbon, the fibers were incredibly thin, extraordinarily long, and exhibited the same symmetry and regularity found in crystalline materials. Later termed carbon nanotubes (CNTs), Iijima’s fibers would soon become the focus of intense scientific research around the world.

While Iijima’s initial observations in 1991 were of multi-walled carbon nanotubes (MWNTs), it was not until 1993 that single-walled carbon nanotubes (SWNTs) were
discovered [39]. Though structurally similar to one another (MWNTs are comprised of several concentric SWNTs of differing diameters) the discovery of SWNTs was an important milestone. Since SWNTs are structurally more fundamental than MWNTs, it became possible to conduct the sensitive experiments on a single nanotube shell which were needed to validate numerous theoretical studies and predictions.

Perhaps the most intriguing prediction was the hypothesis that electrical properties of nanotubes are governed entirely by their geometrical structure [40-42]. First postulated in 1992 and confirmed experimentally in 1998 [43, 44], this theory predicted that the diameter and orientation of the hexagonal lattice with respect to the nanotube axis (chirality) were responsible for determining whether a nanotube was metallic or semiconducting. However, early attempts at CNT synthesis did not adequately control diameter or chirality distributions, thus producing a wide assortment of CNTs with vastly different electrical characteristics.

The next breakthrough towards the eventual incorporation of CNT emitters in field emission devices came in 1996 when a group at Rice University successfully synthesized high quality SWNTs using laser vaporization of a graphite target [45]. Though primarily considered a major leap towards producing high quality CNTs in bulk, the success of the Rice group also initiated a major research effort to better control the CNT diameter and chirality distribution during synthesis. The ability to
differentiate nanotubes with specific geometries is essential for electronics applications since the electrical properties of the nanotubes, and thus the functionality of the device, depend on the chirality. This is particularly true for CNT-based field effect transistors (CNT-FETs), whose performance relies heavily on the semiconducting characteristics of each individually contacted nanotube [24-26].

The final development that would ultimately pave the way for CNT emitters was the capability to grow nanotubes in specific locations and directions using chemical vapor deposition (CVD) [46-52]. Other techniques, such as arc discharge and laser ablation, are not capable of producing the very clean, well-aligned CNTs generated by CVD processes. Instead, the CNTs produced by arc discharge and laser ablation are randomly oriented and often contain significant amounts of amorphous carbon. Utilizing such CNTs for electronic applications is difficult, typically requiring CNT purification to remove amorphous carbon, dispersal onto a substrate, mapping with an atomic force microscope (AFM), and electrical contact formation necessitating electron beam lithography and metal deposition. Though capable of producing individual high performance devices, the processing does not lend itself to parallel fabrication. In contrast, CVD provides a scalable process suitable for massively parallel device fabrication, thus making it ideal for the production of FEAs and similar field emission devices. As a result, the combination of CVD nanotube growth techniques, lithographic patterning technology, and CNT emitters were a perfect match to produce robust and potentially higher performance field emission devices.
At present, numerous devices incorporating CNT field emitters such as vacuum power switches [53], display technologies [11, 54], gated electron guns [2, 4, 5, 55], x-ray [56] and terahertz radiation sources [57, 58], field emission transistors [59], and amplifiers [60] have been, or are being developed.
3 Carbon Nanotubes

3.1 Electronic Structure of Carbon Nanotubes

Having diameters frequently less than 10 nm, carbon nanotubes are a unique class of materials that fall into the size range where quantum effects become important. These structures consist of two-dimensional sheets of crystalline graphite (graphene) that have been rolled up to form seamless one-dimensional cylinders with exceptionally small diameters. Each individual nanotube may contain a single sheet of rolled up graphene, forming a single walled carbon nanotube (SWNT), or numerous graphene sheets, forming a multi-walled carbon nanotube (MWNT). Since carbon nanotubes are constructed entirely from these fundamental graphene sheets, it is only logical to first examine the electronic structure of graphene. With an understanding of the electronic structure of graphene, the consequences of rolling the sheet into a cylinder can be examined and the electronic structure of carbon nanotubes derived.

3.1.1 Electronic Structure of Graphene

In addition to being the building blocks for carbon nanotubes, graphene sheets, when stacked on one another, form graphite. This material has highly anisotropic electronic properties. Electron transport within the individual graphene planes is large, due to pi-orbital overlaps on adjacent atoms in the lattice. However, electron transport between the graphene layers is minimal since the pi-orbital overlap is
small, thus the resistance is large. Using this assumption, P. R. Wallace performed the first detailed band structure calculation for graphite in 1947 [61]. In his work, Wallace assumed that the conduction between the planes was negligible and proceeded to calculate the band structure considering only the in-plane conduction. The details of his work are beyond the scope of this research, thus only the result will be stated here. According to Wallace, the energy of an electron at a point specified by the wavevectors $k_x$ and $k_y$ is given by

$$E_{2Dg}(k_x, k_y) = \pm \gamma_0 \left[ 1 + 4 \cos \left( \frac{\sqrt{3} k_x a}{2} \right) \cos \left( \frac{k_y a}{2} \right) + 4 \cos^2 \left( \frac{k_y a}{2} \right) \right]^{\frac{1}{2}}$$

Equation 1

where $\gamma_0$ is the nearest neighbor transfer integral and $a=2.46$ Å is the in-plane lattice constant.

Applying the result given in Equation 1 to 2D graphite produces both bonding ($\pi$) and anti-bonding ($\pi^*$) pi bands. The two pi bands, shown in Figure 3A, just touch only at the K points (red circles) of the hexagonal graphene Brillouin zone (Figure 3B). The shaded mesh plot of Figure 3A represents a 3D view of the Brillouin zone while the inset gives the $E$-$k$ relationship along the high symmetry points $\Gamma$, K, and M.
Since there is no overlap between the two bands, at zero Kelvin the bonding $\pi$ band will be completely full while the anti-bonding $\pi^*$ band will be completely empty. This can be shown in Figure 4 which illustrates the density of states near the Fermi level for 2D graphite.

Since the density of states near the Fermi level is zero, the graphene sheet can be classified as a zero-gap semiconductor based on Wallace’s calculations. However, in reality graphite is not a zero-gap semiconductor. This was verified in the 1950s when the full 3D graphite band structure was calculated by Slonczewski, Weiss, and McClure [64, 65]. The results indicated that the interaction between the graphene
sheets in 3D graphite cause a slight band overlap of about 40 meV, making graphite a semi-metal having free carriers at all temperatures.

3.1.2 From Graphene to Carbon Nanotubes

To create a single walled carbon nanotube from a 2D graphene sheet, two crystallographically equivalent sites on the hexagonal lattice must be joined. By joining point $B$ with $B^*$ and $O$ with $A$, shown in Figure 5, a nanotube is constructed.

The rectangle denoted by $OBBA^*$ forms the unit cell of the carbon nanotube, the chiral vector, $C$, is defined by the vectors $OA$ and $OB$, and the vector, $T$, is defined as the unit vector of the carbon nanotube. The chiral angle, $\theta$, is defined as the angle between $OA$ and the real space unit vector $a_1$, and adopts values in the range of $0^\circ \leq \theta \leq 30^\circ$ due to the symmetry of the 2D hexagonal lattice.

![Figure 5: The 2D graphene lattice structure with vector notation [62, 66].](image)

To fully describe a carbon nanotube, $C$ is defined by real space unit vectors $a_1$ and $a_2$ such that $C = na_1 + ma_2 \equiv (n,m)$ where $n$ and $m$ are integers and $(0 \leq |m| \leq n)$. The real space unit vectors are given by
where \( a \) is the graphene lattice constant of 2.46 Å \([62, 67]\). The lattice constant, \( a \), is related to the carbon-carbon bond length by \( a = \sqrt{3} a_{c-c} \) where \( a_{c-c} \) is 1.44 Å. Using this construction, three distinct types of nanotubes, zig-zag, armchair, and chiral, can be generated by rolling up the 2D graphene sheet in various directions. In considering just the chiral angle for nanotube classification, only angles satisfying \( 0<\theta<30° \) must be taken into account due to the symmetry of the lattice. The armchair nanotube (Figure 6A) and zig-zag nanotube (Figure 6B) correspond to chiral angles of \( \theta=30° \) and \( \theta=0° \) respectively, while chiral nanotubes (Figure 6C) have a chiral angle of \( 0<\theta<30° \). Note that the names armchair and zig-zag are based on the shape of the ends of the CNT (Figure 6).

Figure 6: The three possible types of carbon nanotubes classified according to chiral angle, \( \theta \). (A) Armchair nanotube with chiral angle of 30°, (B) Zig-zag nanotube with chiral angle of 0°, (C) Chiral nanotube with chiral angle of \( 0° \leq \theta \leq 30° \) [produced using software “Nanotube Modeler”].
Though each nanotube has essentially the same cylindrical shape regardless of its classification, the slight differences in diameter and helicity among the nanotubes plays a crucial role in determining the electronic structure. Prior to experimental verification, theoretical calculations had suggested that the electronic properties of carbon nanotubes were incredibly sensitive to geometry [68-70]. The theory suggested that despite graphene being a zero-gap semiconductor, carbon nanotubes can be either metallic or semiconducting with varying energy gaps depending sensitively on the diameter and helicity (i.e. the indices \( n,m \)). This remarkable relationship between nanotube geometry and electronic properties is due to the quantization of the electron wave vector along the circumference of the nanotube and the unique band structure of graphene, which has electronic states crossing the Fermi level at only two points in \( k \)-space. When determining the electronic structure of graphene, it is assumed that the graphene planes extend infinitely in two dimensions, thus periodic boundary conditions are applied to complete the calculation. For carbon nanotubes, this assumption is not valid since the nanotube, though macroscopic along its axis, has atomic dimensions along its circumference. As a result, the electronic structure is determined using periodic boundary conditions with a period equal to the circumference of the nanotube. Since the circumference is small, the number of allowed states will be very limited.
The permitted electronic states along the nanotube circumference can be thought of as lying on a series of parallel cutting lines within the 2D graphene Brillouin zone (Figure 7). As was discussed earlier, graphene is a zero-gap semiconductor having an empty $\pi^*$ band and an occupied $\pi$ band that intersect only at the K points of the Brillouin zone. As a result, if the cutting lines representing the allowed electronic states intersect with a K point, then the nanotube is considered metallic. If the cutting line does not include a K point then the nanotube will be semiconducting with a band gap dependent on the chirality.

**Figure 7:** (Left) A k-space representation of the 2D Brillouin zone for graphene showing the high symmetry points. (Center) Also shown are the allowed k-states due to the circumferential quantization of the electron wavevector for a semiconducting and a (Right) metallic carbon nanotube.

The metallicity of the carbon nanotubes can also be related to the indices, $(n,m)$. The general rules are: $(n,n)$ nanotubes are metallic, $(n,m)$ nanotubes with $n-m = 3j$, where $j$ is a nonzero integer are semiconducting nanotubes with very small energy gaps, and all other nanotubes are semiconducting with comparatively large energy gaps [62, 66].
3.2 Synthesis and Growth Mechanisms

Carbon nanotubes can be produced using several different techniques, including electric arc discharge between carbon electrodes, laser ablation from a carbon target containing metal catalysts, and various chemical vapor deposition (CVD) processes. The resulting structures are essentially one-dimensional cylinders that exhibit some very remarkable properties. In particular, the geometric property of a high aspect ratio coupled with high mechanical strength and chemical stability make carbon nanotubes incredibly useful as field electron emitters. Additionally, CNTs show remarkable potential to become the central elements in field effect transistors (and other similar devices), and have even been suggested as a medium for high capacity hydrogen storage. However, the potential for CNT devices will not be realized until an optimized and controllable growth process is developed.

Most real-world applications of CNTs require large quantities of CNTs, typically of a very high quality or particular geometric structure. For approaches such as polymer reinforcement and high capacity hydrogen storage, large quantities (typically 100s of kilograms) of high quality CNTs are required. At the other extreme, CNT-based electronic devices will have to rely on self-assembly of CNTs or controlled growth schemes combined with microfabrication techniques to mass produce functional devices.
3.2.1 Arc Discharge and Laser Ablation

To fulfill the potential of CNT based devices, growth techniques must be developed that can produce high quality SWNTs and MWNTs while controlling the diameter distribution and chirality during the growth process. Since the chirality and diameter essentially dictate electrical characteristics of the CNTs, controlling these parameters during the growth process will be desirable in bringing the promise of CNT devices to fruition. To combat these technical hurdles, much scientific research has been devoted to the study of CNT growth over the past decade. Two of the first growth techniques used to synthesize CNTs were arc discharge and laser ablation.

Despite the fact that arc discharge and laser ablation differ in their respective approaches, the end goal remains the same. Both techniques seek to heat a carbon target to 3000°C-4000°C in order to vaporize and subsequently condense the carbon atoms to form CNTs. In an arc discharge system the thermal energy is provided by a helium plasma that is initiated between opposing carbon electrodes by high currents (Figure 8A). This particular method can produce both high quality multi-walled and single-walled nanotubes simply by varying parameters such as the gas pressure in the chamber and the magnitude of the arcing current. The resulting CNTs from the arc discharge process typically have lengths measured in 10s of microns and diameters ranging from 5-30 nm [62]. They also exhibit a high degree of crystallinity as evidenced by their overall straightness suggesting a very low defect density. One of the drawbacks of arc discharge is that the as-produced CNTs are often contaminated
with multi-layered graphitic particles that adopt polyhedron morphologies. Though this contamination can be removed by thermally oxidizing the byproducts, a significant percentage of the desirable CNTs are also destroyed in the process.

![Schematic experimental configurations of both (A) electrical arc discharge and (B) laser ablation methods for CNT synthesis.](image)

Although similar to arc discharge, laser ablation utilizes intense laser pulses to ablate a carbon target that often contains trace amounts of metal catalysts such as cobalt or nickel. During the ablation process, argon gas passes through a tube furnace heated to 1200 °C to provide an inert environment and to carry the synthesized CNTs downstream to a collector (Figure 8B). The resulting CNTs are often found in bundles that are 10-20 nm in diameter and as long as 100 μm or more in length [62, 66]. Like arc discharge, changes to parameters such as growth temperature and catalyst composition can vary the nanotube diameter and diameter distribution. Laser ablation techniques also typically show carbon contaminants similar to arc discharge methods.
Though arc discharge and laser ablation have been the primary methods used to produce high quality CNTs, there are some issues relating to these methods. Both methods require the heating of solid carbon sources in excess of 3000°C, which is inefficient and limiting to the scalability of CNT production. The as-produced CNTs from each approach also occur in bundles thus making purification, manipulation, and assembly into functioning devices difficult. Moreover, contaminants such as fullerenes, amorphous carbon (either as particles or a coating on the CNT sidewalls), and metal catalyst particles are also common and must be removed.

In order for the as-produced CNTs from both arc discharge and laser ablation to be applicable to CNT based electronics, a technique to deposit the CNTs at specific locations must be developed and optimized. Serial approaches using AFM manipulation are certainly not practical. Electrical manipulation techniques such as dielectrophoresis [71-76] are promising due to their parallel approach, but currently lack the ability to sort CNTs by chirality. CNT based devices will certainly require nanotubes with specific electronic properties, necessitating a method for reliably sorting CNTs by chirality and diameter. Some attempts have been made [73, 77]; however, more research must be completed before separation techniques are optimized and ready for large scale use.

3.2.2 Chemical Vapor Deposition

While laser ablation and arc discharge are able to produce bulk quantities of high quality CNTs for study, the problem remains of assembling these CNTs in a useful
manner to produce functioning CNT-based electronic devices. Techniques such as direct AFM manipulation and electron beam lithography, while successful, are not suitable for parallel processing, a criterion that will undoubtedly have to be met. Dielectrophoresis shows much promise, but also has its own set of challenges. A potential solution for producing CNT-based devices without depending on serial processes is chemical vapor deposition (CVD). CVD methods are advantageous because the CNTs only grow from the metal catalyst particles, which are typically iron, cobalt, or nickel. Additionally, they grow at significantly lower temperatures, typically 500-1000°C, as compared to arc discharge and laser ablation. When CVD methods are combined with lithographically patterned catalyst thin films, selective growth and assembly of CNTs can be achieved. The result is a simplified, and most importantly, scalable approach for assembling CNT-based electronic devices.

A schematic experimental setup of a typical thermal CVD growth is shown in Figure 9. The thermal CVD growth process involves the heating of a transition metal catalyst, typically iron, cobalt, or nickel, to high temperatures (500-1000°C) in the presence of a hydrocarbon gas. As a result, CNTs will grow only from the metal catalyst particles. The generally suggested growth mechanism of the CNTs by thermal CVD begins with the dissociation of the hydrocarbon gas catalyzed by the transition metal. Following the dissociation, the gas dissolves into the catalyst until the particle becomes saturated. At this point, the carbon precipitates out of the particle and forms tubular structures. Tubular structures are the favored morphology
due to a minimization of dangling carbon bonds, resulting in a low energy configuration [62, 66].

Thermal CVD can produce both MWNTs and SWNTs, however, the processes involved in producing each type of CNT differs greatly. To produce MWNTs, the most commonly used hydrocarbon gases are ethylene [46, 48, 78] or acetylene [51, 52, 79, 80] and require furnace temperatures of 550-750°C. To produce SWNTs higher temperatures are required, typically ranging from 850-1000°C, while the hydrocarbon source is usually methane [47, 50, 81, 82]. High temperature is needed to produce SWNTs since they have smaller diameters, and hence greater strain energies, when compared to MWNTs. The higher temperature of SWNT growth also helps to anneal out defects thus enabling the formation of nanotube structures with a higher degree of crystallinity. Methane is used for SWNT synthesis since it is more stable against self-decomposition at high temperatures as compared to the other hydrocarbon gases. As a result, the methane primarily dissociates from the catalytic action of the transition metal rather than due to self-decomposition.
Although thermal CVD offers the ability to grow ordered and aligned nanotube structures not possible with arc discharge and laser ablation, there are some disadvantages. First, the MWNTs produced by thermal CVD typically have higher defect densities when compared to the as-produced MWNTs from arc discharge and laser ablation. This is due mostly to the lower processing temperature, which is not hot enough to fully anneal out defects that may form during growth. Conversely, nearly perfect SWNTs are possible by thermal CVD, though the temperature must be increased significantly. The temperatures used in both SWNT and MWNT thermal CVD synthesis ultimately dictate its integration with a fabrication process in device production. Delicate devices, polymer layers, multilayer thin films, and photoresists are examples of structures and materials that will likely suffer some degradation or even total failure when raised to the typical growth temperatures of thermal CVD.

### 3.2.3 Plasma Enhanced Chemical Vapor Deposition

Due to the high processing temperatures, techniques incorporating plasmas into the CVD process (known as plasma enhanced CVD - PECVD), have been developed that permit the synthesis of carbon nanotubes at lower temperatures compared to thermal CVD methods. Such techniques include rf-PECVD [83], microwave PECVD [84], inductively coupled PECVD [85], and dc glow discharge PECVD [86]. While thermal CVD typically employs temperatures of 700-1000°C for CNT synthesis, plasma CVD techniques typically operate between 600-700°C. The additional energy necessary to grow CNTs comes from the energy present in the plasma discharge of the system.
Figure 10: SEM image showing CNTs synthesized (A) without plasma and (B) with plasma. The CNTs synthesized without the plasma adopt a spaghetti-like orientation while the CNTs synthesized with the plasma are highly aligned to the electric fields present during the growth [87].

In addition to lowering the processing temperature, plasma CVD also has another advantage over thermal CVD in that the CNTs align to the electric fields in the chamber during the growth. These fields are normal relative to the substrate surface so the results are very straight, highly ordered CNT films, shown in Figure 10B. In comparison, when a plasma is not used, no electric fields are present and the CNTs adopt a random, spaghetti-like orientation (Figure 10A). This ability to not only grow CNTs but to control their orientation using electric fields is an important advantage of plasma CVD over thermal CVD. However, more recent studies have also demonstrated the ability to use standard thermal CVD synthesis to fabricate densely packed, horizontal arrays of highly aligned CNTs [88].

### 3.2.4 Growth Mechanisms

Despite the tremendous progress in CNT synthesis techniques, an understanding of the underlying growth mechanisms has lagged significantly and remains controversial to this day. The inaccessibility of the synthesis process makes it very
difficult to directly observe the nanotube growth and the associated growth mechanisms. One proposed theory assumes that the growing CNTs are capped and grow through a $C_2$ absorption process aided by the pentagonal defects present on the CNT caps [89]. Others believe that the CNTs are open ended during the synthesis process and carbon atoms are added at these locations giving rise to CNT growth [90, 91]. It is important to note that due to the widely varying conditions for each specific growth process there may be more than a single growth mechanism at work. At present, a full understanding of the growth model for carbon nanotubes remains incomplete. To realize the full potential of carbon nanotubes as an electronic material a deeper understanding of the growth mechanism(s) is needed. By further understanding the growth kinetics, processes capable of controlling diameter and chirality may ultimately be possible. Such processes would greatly advance the prospects for large scale CNT device production as they provide a means for producing geometrically, and thus, electronically similar CNTs.

### 3.3 Summary of Physical Properties

Since being discovered in 1991, much research has been done exploring the unique properties of carbon nanotubes. As has already been discussed, despite the similarities between carbon nanotubes and 2D graphite, graphene is a zero gap semiconductor at room temperature while carbon nanotubes can be either metallic or semiconducting, depending on the diameter and chirality. Carbon nanotubes can also be either single-walled or multi-walled, referring to the number of concentric
cylinders present in the structure. Due to the weak coupling between the concentric cylinders, the electronic properties of multi-walled nanotubes and single-walled nanotubes are very similar. Conduction in both species of carbon nanotubes occurs ballistically over macroscopic distances. This implies that carriers experience very little scattering during conduction, thus carbon nanotubes are able to carry very large currents with significantly less heating than other materials. Similar to carrier transport, phonon propagation in carbon nanotubes is also excellent with individual multi-walled nanotubes demonstrating thermal conductivities greater than 3000 W/m·K which is higher than both natural diamond and the basal plane of graphite [92]. Carbon nanotubes also exhibit remarkable structural properties. Single-walled carbon nanotubes with small diameters have a high Young’s modulus and high tensile strength exceeding that of steel wire [93].

The relative size of a carbon nanotube diameter compared to its length, also known as the aspect ratio, gives rise to a unique geometric property. The geometric property of a high aspect ratio coupled with high mechanical strength and chemical stability make carbon nanotubes incredibly useful, especially as electron emitters in field emission devices. Despite having a work function of ~5 eV, which is comparable to graphite, carbon nanotubes are attractive field electron emitters due to the large electric field enhancement found at their tips while under low macroscopic fields between anode and cathode. Because of this geometrically related electric field enhancement, the electric fields in the vicinity of the carbon nanotube tips can
increase by $10^2 - 10^3$ V/µm. The high local enhancement of the electric field permits the carbon nanotubes to reach the field emission threshold at lower macroscopic fields compared to devices using other emitting structures such as conical metal tips. Table 2 shows a general comparison of carbon nanotube emitters to other commonly used field emitter materials.

Table 2: Threshold electric field values for various materials for a current density of 10 mA/cm² [94, 95].

<table>
<thead>
<tr>
<th>Material</th>
<th>Threshold electrical field (V/µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Molybdenum tips</td>
<td>50 – 100</td>
</tr>
<tr>
<td>Silicon tips</td>
<td>50 – 100</td>
</tr>
<tr>
<td>p-type semiconducting diamond</td>
<td>130</td>
</tr>
<tr>
<td>Undoped, defective CVD diamond</td>
<td>30 – 120</td>
</tr>
<tr>
<td>Amorphous diamond</td>
<td>20 – 40</td>
</tr>
<tr>
<td>Cesium coated diamond</td>
<td>20 – 30</td>
</tr>
<tr>
<td>Graphite powder (&lt; 1 mm size)</td>
<td>17</td>
</tr>
<tr>
<td>Nanostructured diamond (heat-treated in H₂ plasma)</td>
<td>3 – 5 (unstable &gt; 30 mA/cm²)</td>
</tr>
<tr>
<td>Carbon nanotubes (random film)</td>
<td>1 – 3 (stable at 1 A/cm²)</td>
</tr>
</tbody>
</table>

Individual carbon nanotubes have also shown excellent electron transport properties with a single nanotube capable of stably emitting currents up to 1 µA [96]. When arranged as a randomly oriented film, often after a CVD growth, the current densities from CNTs have been shown to be on the order of Amps/cm² without seeing any significant degradation of the CNT film [12].

These remarkable properties of carbon nanotubes make them very attractive for numerous electronic devices including sensors [56, 93, 97, 98], thin film transistors [21, 25, 99], electron emission sources [2, 11, 56, 100-102], and device interconnects.
[103-105], among others. These nanometer sized cylinders have the right combination of properties – small size, high aspect ratio, high strength, chemical stability, and high conductivity – that make them so versatile, and so intriguing for electronic devices and materials. While the applications for carbon nanotubes are varied, this work will focus on utilizing them as field emitters in a unique, lateral device geometry and the techniques and processes needed to create such devices.
4 Field Electron Emission

4.1 Historical Background

Although the phenomenon of field emission was first described by Robert W. Wood in 1897 while conducting experiments using a discharge tube [106], it was the development of quantum mechanics during the early 1900s that led to a more rigorous theoretical and ultimately experimental understanding. In 1928, using the new quantum theory, Ralph Fowler and L. W. Nordheim successfully calculated a relationship between the field emitted current density and the applied electric field based on the tunneling of electrons through a 2D triangular barrier [107, 108]. However, verifying the predictions of Fowler and Nordheim experimentally proved challenging since obtaining reproducible field emission was difficult at the time. High voltages made the experimental systems prone to arcing, but the major issue was the invisible microstructure of the emitting material and its strong effect on the emission characteristics.

Following the initial work by Fowler and Nordheim numerous other contributions were made to the topic of field emission. In 1937, Müller created a finely etched tungsten wire and placed it in the center of a glass sphere which had a fluorescent material coating the inside surface. After applying an electric field, Müller observed a symmetric fluorescent pattern resulting from field emitted electrons coming from the tungsten tip. Müller would eventually go on to verify the earlier work of Fowler
and Nordheim over a wide range of currents and voltages with the help of Good, Dyke, and Dolan [109]. Furthermore, the work done by Müller and his co-workers would eventually become the foundation for the modern field emission microscope.

4.2 Fowler-Nordheim Discussion

Field emission is the emission of electrons into vacuum, via strong applied electric fields, whose mechanism depends entirely on quantum mechanical tunneling. The reason field emission can occur is due to the wave nature of the electron, as proposed by deBroglie in 1924 and verified in 1927 by Davisson and Germer [110]. This phenomenon arises from the electron wavefunction failing to vanish at the potential barrier and instead undergoing an exponential decay as it travels into, and ultimately, through it. As a result, the electron is emitted into the vacuum despite having significantly lower energy than that of the barrier. This differs greatly from other electron emission mechanisms such as thermionic and photoelectric emission. In these processes, the electron can pass over the potential barrier (Figure 11A and B) and into the vacuum by acquiring additional energy, usually imparted by heating or incident photons.

Figure 11 illustrates a metal at low temperature having electrons occupying all states up to the Fermi level, denoted by $E_F$. Slightly above the Fermi level, typically by a few electron-volts, is the vacuum level. The vacuum level represents the potential of an electron found at rest outside the metal in a region free of external electric fields.
The difference between $E_F$ and the vacuum level is referred to as the work function, given by $\varphi$, and is the amount of energy an electron would need to escape into the vacuum by passing over the potential barrier. Under these conditions all of the electrons remain within the metal unless sufficient energy is added.

![Figure 11: Energy level schematic illustrating field electron emission from a metal showing the potential barrier (A) before and (B) after application of a strong electric field.](image)

If a large electric field is now applied, the potential outside the metal will become deformed and adopt a triangular shape (Figure 11B). If the barrier is reduced, or “thinned” sufficiently, the electrons will tunnel through given that their wavefunctions do not decay to zero before reaching the other side. The electrons that are emitted should also have a relatively small energy spread since most originate from a narrow region around the Fermi level, where the barrier is the thinnest.

### 4.2.1 Theory

The relationship between the field emitted current density and the applied electric field was first formulated by Fowler and Nordheim in 1928 [107, 108]. According to
modern Fowler-Nordheim (F-N) theory for a 1D system with a planar electrode configuration, the emission current density can be written as

\[
J = \frac{B}{t^2(y) \phi} F_0^2 \exp \left( - \frac{C \phi^{3/2}(v(y))}{F_0} \right)
\]

Equation 3

where \( J \) is the current density in \([A/m^2]\), \( F_0 = V/d \) is the electric field between the electrodes in \([V/m]\), \( V \) is the applied voltage in \([V]\) and \( d \) is the distance separating the electrodes in \([m]\). The work function of the emitting material is \( \phi \) and given in \([eV]\). The terms \( B \) and \( C \) are field independent constants and are defined as

\[
B \equiv 1.5414 \times 10^{-6} [A \cdot eV \cdot V^{-2}], \quad C \equiv 6.8309 \times 10^9 [eV^{-3/2} \cdot V \cdot m^{-1}]
\]

Equation 4

Both \( t(y) \) and \( v(y) \) are dimensionless electric field dependant elliptical functions that are taken to be unity.

Equation 3 gives the current density as a function of the applied electric field (and hence voltage and electrode separation) and the work function of the emitting material. However, this formulation deals with an idealized parallel plate configuration lacking micro- and nanostructure at the electrode surfaces. In reality,
all surfaces, no matter how smooth, have some roughness at the micro- or nanoscale. The presence of this roughness greatly affects the electric field near the emitting surface. This is due to the ability of a small, protruding asperity to concentrate and enhance the electric field near its tip. Figure 12 illustrates the mechanism of geometrical electric field enhancement. Here, the field emission between two parallel plates without any field enhancement is shown at left. In this ideal case, the field emission would be uniform across the surface of the cathode due to equal electric field strength along its length. However, if a high aspect ratio structure exists on the cathode, shown at right, then the electric field is enhanced locally around the tip of the structure. This results in much higher local electric fields and causes the field emission to originate from the high aspect ratio structure.

![Figure 12](image_url)

Figure 12: (Left) Idealized parallel plate field emission configuration lacking electrode surface roughness, thus the electric field is uniform. (Right) Electrode having protruding asperities that concentrate and enhance the electric field strength in the vicinity of the tip apex.
The higher the aspect ratio of the asperity, the larger the electric field enhancement will be. As a result, the macroscopic electric field for a parallel plate configuration, \( F_0 \), will be much smaller than the local electric field, \( F_{loc} \), at the tips of individual asperities.

To determine the magnitude of the field enhancement factor, denoted by \( \gamma \), the electric field at the emitter tip, \( F_{loc} \), must first be determined. According to simulations performed by Edgecombe and Valdre, for a cylindrical emitter with a planar anode the electric field enhancement factor takes the functional form [111]

\[
\gamma \approx 1.2 \left( \frac{L}{r} + 2.15 \right)^{0.90}
\]

Equation 5

where \( L \) and \( r \) are again the length and radius of the emitter, respectively. While a useful simulation, this formulation applies primarily to single emitters, such as Spindt cathodes or individual carbon nanotubes. When obtaining field emission from carbon nanotubes, the emission often originates from an array of nanotubes and not a single emission site. Factors such as the geometry distribution (diameter and length) of the nanotubes and electric field screening effects are not accounted for in this simulation. Thus, it is better to obtain the field enhancement factor from experimental data rather than estimates of nanotube geometries.
To complete the analysis, the field enhancement factor, $\gamma$, is related to the local electric field, $F_{loc}$, and the macroscopic field, $F_0$, by the following.

$$F_{loc} = \gamma F_0 = \gamma \frac{V}{d}$$

**Equation 6**

Combining Equation 6 with Equation 3, the expression for the current density can be written as

$$J = \left( \frac{B}{\phi} \right) (\gamma^2 F_0^2) \text{Exp} \left( -\frac{C\phi^{3/2}}{\gamma F_0} \right)$$

**Equation 7**

In determining the current density, $J$, the area of the emitting surface (cathode) is used. For the purpose of this research, Equation 7 will prove sufficient in analyzing the field emission from the carbon nanotubes in the electronic devices. Further refinements to the Fowler-Nordheim theory have been performed [112-114]; however, they are beyond the scope of this work.

### 4.2.2 Coordinates and Enhancement Factor

To determine the field enhancement factor experimentally, the current-voltage (I-V) data must be used in conjunction with Equation 7, which suggests that if one plots
\( \ln\left(\frac{J}{F^2}\right) \) as a function of \( 1/F \) for field emission data, the corresponding curve should follow a straight line with a negative slope. The resulting data plot is typically referred to as a Fowler-Nordheim plot and the coordinates, \( \ln\left(\frac{J}{F^2}\right) \) and \( 1/F \), as Fowler-Nordheim coordinates. From the Fowler-Nordheim plot, an estimate of the field enhancement factor is readily obtained. Since the equation of a line has the form \( y = mx + b \), Equation 7 can be rewritten as follows

\[
\ln\left(\frac{J}{F_0^2}\right) = \ln\left(\frac{B\gamma^2}{\phi}\right) - \frac{C\phi^{3/2}}{\gamma} \frac{1}{F_0} 
\]

Equation 8

From Equation 8 the slope and y-intercept of the plot are easily distinguished and are given by

\[
|m| = \frac{C\phi^{3/2}}{\gamma} 
\]

Equation 9

\[
b = \ln\left(\frac{B\gamma^2}{\phi}\right) 
\]

Equation 10
Although the field enhancement factor, $\gamma$, appears in both the slope and y-intercept, it is simpler to use the slope to determine its value. Solving Equation 9 for the field enhancement factor yields the following relation

$$|m| = \frac{C \phi \gamma}{\gamma} \rightarrow \gamma = \frac{C \phi \gamma}{|m|}$$

Equation 11

Using Equation 11 with a linear fit of the F-N data plot will readily yield an estimate for the electric field enhancement present at the emitter tips.

Carbon nanotubes are naturally well suited to be excellent field emitters mainly due to the fact they are inherently high aspect ratio structures. By possessing nanometer scale diameters, and comparatively macroscopic lengths, typically on the order of microns, carbon nanotubes are ideal one-dimensional conductors. The small tip radii of carbon nanotubes also present the opportunity for extremely large electric field enhancement near the tip apex. The increased local electric fields at the CNT emitter tips enables device operation at comparatively lower voltages since smaller anode-cathode voltages are capable of reaching the emission threshold.
5 Dielectrophoresis

5.1 Background and Importance

Since they were discovered by Iijima in 1991 [38], carbon nanotubes have been researched extensively. This interest has been motivated primarily by the potential applications of CNTs, particularly SWNTs, into nanoscale electronic devices based on their unique electronic properties and nanometer sizes [21, 22, 25-27, 99]. SWNTs are more desirable over their multi-walled cousins because SWNTs provide a nearly perfect model of a one-dimensional conductor since a SWNT contains only a single graphene shell. In addition, SWNTs have demonstrated astounding properties at room temperature, often exceeding the performance of semiconductor materials under the same conditions [115-117]. These fundamental studies on SWNTs have revealed charge transport mobilities an order of magnitude larger than that of silicon and maximum current carrying capacities on the order of $10^9$ A/cm$^2$ [66]. The implications of these characteristics are significant for numerous applications in electronics, sensors, and other such technologies.

Though the physical and electronic characteristics of single SWNTs are impressive, it is still questionable whether single-SWNT devices can provide a realistic foundation for future technologies. Single-SWNTs are limited to currents of order 1 μA [96] and their nanometer size results in minute active regions, potentially making integration into sensing platforms difficult. However, the more formidable
technological hurdle facing single-SWNT devices is the lack of precise CNT manipulation and assembly techniques. The solution to this problem is complex, as are the requirements needed to make CNT based devices a reality. Any potential solution must be capable of accurately synthesizing and positioning large numbers of electrically homogeneous CNTs. At present, synthesis methods for producing high quality CNTs with low defect densities have been developed for both SWNTs and MWNTs using laser ablation and arc discharge techniques [45, 47, 50, 66, 118]; however, the positioning technology has lagged behind. One current method for CNT manipulation uses an atomic force microscope (AFM) tip [21, 119] physically moving the CNTs into the desired orientations. Electron beam (e-beam) lithography and thin film deposition methods are then used to create electrical contact to the CNT. Though the AFM / e-beam lithography combination offers precise control over CNT orientation and contact, the two processes are an impractical long-term solution for CNT device fabrication due to a lack of scalability.

Although the future of single-SWNT based devices remains uncertain, the potential for devices relying upon CNT bundles or thin films is much more plausible. A bundle or thin film of CNTs would satisfy the demands for increased device currents as well as increase the active area for sensing applications. Therefore, the method used to create the CNT thin film must be capable of producing a high quality CNT film that is densely packed, highly aligned, scalable, and ideally occurs at room
temperature. A potential technique addressing these issues is dielectrophoresis [120, 121].

Dielectrophoresis is based on the fundamental interaction between matter and electric fields. When a particle is placed in an alternating electric field, a time dependent polarization is induced in the particle due to charge redistribution, thus generating a force acting on the particle. If the applied electric field has a nonzero spatial gradient (a non-uniform field) then the particle will experience a net force resulting in translational motion whose magnitude and direction will depend on the physical properties of the particle and suspending medium.

![Figure 13: Circuit schematic illustrating a typical experimental setup for performing dielectrophoresis on carbon nanotubes. Depending on the dielectric properties of the CNTs and suspending medium, the CNT will align to the applied field and either be attracted to or repelled from regions of increasing electric field strength.](image)

In the case where the particle is more polarizable than the suspending medium, as shown in Figure 13, then the dipole aligns to the field and moves in the direction of increasing electric field strength. In the case where the particle is less polarizable than the medium then the dipole aligns against the field and moves in the direction of
decreasing electric field strength. Attraction to regions of highest electric field is known as positive DEP while repulsion from such regions is known as negative DEP.

5.2 Theoretical Discussion

For an uncharged particle, such as a carbon nanotube, with dipole moment $\mu$, polarizability $P$, and placed into a non-uniform electric field, $E$, the dielectrophoretic force on that particle is given by

$$F_{\text{DEP}} = P \cdot (\nabla E) = \mu (E \cdot (\nabla E))$$

Equation 12

For DEP, only situations where the electric field has a component parallel (or anti-parallel) to the gradient need to be considered since only those situations will produce a net force on the dipole. Components of the electric field perpendicular to the gradient do not produce a net force on the dipole. For a cylindrical particle (CNT) the dielectrophoretic force acting on that body is given by the following [122-124]

$$F_{\text{DEP}} = \Gamma \varepsilon_m \text{ Re} [K(\omega)] \nabla E^2$$

Equation 13
where $\Gamma$ is a geometric factor, $\varepsilon_m$ is the permittivity of the suspending medium, $E$ is the root-mean-square electric field, and $\text{Re}[K(\omega)]$ is the real component of the Clausius-Mossotti factor given by

$$K(\omega) = \frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_p^* + 2\varepsilon_m^*}$$

Equation 14

where $\varepsilon_p^*$ and $\varepsilon_m^*$ are the complex permittivities of the particle and medium respectively, and

$$\varepsilon_{p,m}^* = \varepsilon_{p,m} - j\frac{\sigma_{p,m}}{\omega}$$

Equation 15

with $\varepsilon$ the permittivity, $\sigma$ the conductivity, and $\omega$ the angular frequency of the applied electric field. The subscripts $p$ and $m$ refer to the particle and the medium respectively.

The frequency dependence of $\text{Re}[K(\omega)]$, shown in Equation 14 and Equation 15, suggests that the dielectrophoretic force exerted on the particle will also vary with frequency. In addition, the value of the Clausius-Mossotti factor can adopt both positive and negative values. As a result, the direction of $F_{DEP}$ will depend on the
sign of $\text{Re}[K(\omega)]$ since no other quantities in Equation 13 can take on negative values. The value of $\text{Re}[K(\omega)]$ will depend on whether the particle is more or less polarizable than the suspending medium surrounding it. If $\text{Re}[K(\omega)]$ results in a positive value, the particle will move in the direction of increasing electric field strength. Conversely, if $\text{Re}[K(\omega)]$ results in a negative value, the particle will be repelled from such regions.

In the case of a metallic particle, $\text{Re}[K(\omega)] \approx 1$ due to the constant redistribution of conduction band electrons to reduce the internal electric fields to zero [125]. This implies that for all metallic particles the Clausius-Mossotti factor will always have a positive value, thus metallic particles will always experience positive DEP as shown in Figure 14.

![Figure 14: Plot of the real part of the Clausius-Mossotti factor, $\text{Re}[K(\omega)]$, for metallic and semiconducting particles as a function of the angular frequency of the applied electric field, $\omega$.](image)

For semiconducting particles the physics are slightly more complicated as $\text{Re}[K(\omega)]$ may adopt both positive or negative values depending on the details of the system.
and the angular frequency of the applied electric field. As a result, $F_{DEP}$ can be positive or negative for semiconducting particles. Moreover, this transition point, denoted here as $\omega_t$, should exist at $\text{Re}[K(\omega)] = 0$ and will indicate a crossover from a positive to negative dielectrophoretic force or vice versa (Figure 14).

The same analysis can be performed for carbon nanotubes as they are well-suited for dielectrophoretic manipulation. Carbon nanotubes (both SWNTs and MWNTs) can adopt either metallic (m-CNTs) or semiconducting (s-CNTs) configurations, with each having unique dielectric properties. Since the polarizabilities differ, the magnitude of the dielectrophoretic forces experienced by the m-SWNTs and s-SWNTs in suspension will also vary, and under some conditions be opposite one another. As a result, it should be possible to perform an in-situ separation of metallic and semiconducting nanotubes based on differences in dielectric properties [72-74, 124].

For a semiconducting single-walled carbon nanotube (s-SWNT) the relative dielectric constant has been calculated to be of the form [73, 126]

$$\varepsilon_{s-SWNT} = 1 + \left( \frac{\hbar \omega_{\text{plasma}}}{5.4 E_{\text{gap}}} \right)^2$$

Equation 16
where $\hbar \omega_{\text{plasma}}$ is the energy of the plasma oscillation ($\approx 5$ eV) along the axis of the carbon nanotube [127], and $E_{\text{gap}}$ is the band gap energy. Taking an estimate of the band gap to be on the order of $\sim 1$ eV, the relative dielectric constant for s-SWNTs is approximately 2. Given the range of potential band gaps for a s-SWNT, a range of $1 < \varepsilon < 5$ is appropriate to consider once all the possible band gaps are translated to dielectric constants. In the case of metallic SWNTs (m-SWNTs) a very large value for the dielectric constant is expected due to the presence of mobile charge carriers. Furthermore, research has been done suggesting that the polarizability of m-SWNTs is effectively infinite [126]. This will also be true for some s-SWNTs having band gaps smaller than the thermal energy, $k_B T$, since they will also have mobile charge carriers in the conduction band. For these nanotubes, a positive dielectrophoresis will be derived, while the sign of the dielectrophoretic force for s-SWNTs with band gaps larger than $k_B T$ will depend more on the relative dielectric properties of the s-SWNT compared to that of the suspending medium.

### 5.3 Preparation of Carbon Nanotube Suspensions

For this research I utilized carbon nanotubes that were positioned via dielectrophoresis using a suspension of CNTs. The single-walled nanotubes were purchased commercially (Carbon Nanotechnologies, Inc.) and have lengths of 1 to 10 $\mu$m and diameters of 0.8 to 1.0 nm. The single-walled nanotubes, due to their synthesis, contain amorphous carbon and significant amounts of catalyst particles, which are removed by a common purification process found in the literature [128-
This process involves refluxing the CNTs in concentrated nitric acid at temperatures near 120°C. The purified nanotubes were then placed into the suspension medium, dimethylformamide (DMF). The multi-walled nanotubes were grown by thermal chemical vapor deposition [79, 80, 131] using an acetylene (C$_2$H$_2$) carbon seed gas and a 5 nm thick iron (Fe) catalyst layer evaporated onto thermally oxidized silicon. The multi-walled nanotubes typically had diameters ranging from 20 to 50 nm and lengths from 10 to 20 μm depending on the parameters of the growth process. Following the CVD, the multi-walled nanotubes were removed from the substrate and placed directly into the DMF suspending medium. Single-walled and multi-walled suspensions of 0.5 to 10 μg of nanotubes per milliliter of DMF were used. A stock suspension with a concentration of 100 μg/mL was made, then ultrasonicated using an ultrasonic horn (Misonix Sonicator 3000) for two hours. The sonication process is necessary to help disperse the nanotubes in the suspension by breaking up larger bundles. The stock solution was diluted to 0.5 to 10 μg/mL then sonicated again in the same manner. Prior to each dielectrophoretic deposition, the suspension was sonicated for an additional 60 minutes and passed through a 1.6 μm filter to remove any large nanotube bundles. Confirmation of CNT dispersion is done by allowing some suspension to evaporate on a silicon substrate and then viewing the surface in an SEM.
6 General Overview of Device Concept

The two main goals of this work are to research and develop novel CNT-based field emission diode and triode structures capable of withstanding harsh operating environments and integrating these devices into electronic circuits. Such harsh environments would include high (~500 °C) and low (cryogenic) temperature applications, as well as situations where ionizing radiation is present, such as space exploration, nuclear reactors, and hospital radiology departments. Device fabrication will be completed utilizing standard semiconductor processing techniques.

6.1 Field Emission and Harsh Environment Compliance

Field emission devices are able to operate at high temperatures without any decrease in performance due to the carriers (electrons) being field emitted into a vacuum rather than conducted through a semiconductor. As we can see from the Fowler-Nordheim equation (Equation 7), the relation between emission current and applied field is free from any obvious temperature dependence. The result is an electron emission process minimally affected by temperature. This same statement cannot be made for semiconductor based electronics since device performance in such devices is heavily temperature dependent.
For an intrinsic semiconductor, or a semiconductor free of dopants, the occupation of the conduction band as a function of temperature is proportional to [67]

\[ Exp \left( -\frac{E_g}{2k_B T} \right) \]

Equation 17

where \( E_g \) is the energy gap in [eV], \( k_B \) is Boltzmann’s constant in [eV/K], and \( T \) is the temperature in [K]. At high temperatures, the intrinsic semiconductor’s valence electrons are thermally excited across the energy gap, \( E_g \), and into the conduction band (Figure 15). As suggested by Equation 17, the carrier density in the conduction band increases exponentially with increasing temperature, thus raising the conductivity of the semiconductor. However, modern day devices do not use intrinsic semiconductors, instead relying upon the addition of dopant atoms which drastically alter the electrical characteristics. There are two classifications of dopant
atoms that can be added to change the electrical properties of a semiconductor: donors and acceptors. Donors supply additional electrons to the conduction band and are often Group 5A elements, while acceptors supply additional holes to the valence band and are usually Group 3A elements. As shown in Figure 15, both the donor and acceptor atoms create energy levels that lie very close to the boundaries of the forbidden energy region. With the addition of these allowed states, it becomes far easier to excite an electron from a donor level to the conduction band or a hole from an acceptor level into the valence band than it is to excite an electron or hole across the entire energy gap.

As has been mentioned, with rising temperature, the performance of semiconductor devices begin to degrade and ultimately fail, typically above 300°C for silicon. Field emission devices can operate at much higher temperatures, and are often limited only by material properties and operating environment. There also exist both high and, specifically for bipolar junction transistors (BJTs), low temperature ranges, (material and dopant level dependent) that constrain the operating range of the device. At low temperatures outside the operating range, the charge carriers in a BJT will remain bound to the dopant atoms, while at higher temperatures control over the carrier densities in the conduction band is lost. In each case, the device will not function properly. These same temperature limits also generally hold true for field effect transistors (FETs). At high temperatures, FETs suffer from the same issues as BJTs; however, at low temperatures the application of a gate potential can often bend the
bands enough that the device remains operational. It is important to note that the gate potential cannot be made arbitrarily large in order to keep the device operational since too large a voltage will lead to catastrophic dielectric failure and ultimately the destruction of the FET.

In addition to having minimal temperature dependence, ionizing radiation also has little to no effect on field emission devices since electron transport occurs in vacuum. Since radiation cannot damage or generate charge in vacuum, field emission devices can operate in high radiation environments. At the proposed operating current densities on the order of Amps/cm², electron-radiation interactions would also be negligible. This is not the case for semiconductors since ionizing radiation will mainly affect devices in two ways: physical damage to the conducting channel, and capacitance increases due to the generation of electron-hole pairs. The importance of the physical damage depends upon the width of the conducting channel. In older devices, which have wider channels, a radiation strike resulting in a lattice dislocation or other such defect would have a minimal effect due to the sheer size of the channel. As channel widths have shrunk, it becomes less likely a radiation strike will occur, but in the event one does, the effect would be greater. In general, changes in device performance resulting from physical damage to the channel are minimal and not overly problematic. The bigger issue for semiconductor electronics subjected to ionizing radiation is the generation of electron-hole pairs. The charge generation caused by the radiation can cause voltage changes within the device. In digital
electronics, this can be an issue if the voltage swings are enough to change the digital state of the device.

The issues of temperature and radiation control can certainly be overcome when employing semiconductor based devices; however, there are drawbacks to taking such an approach. Cooling systems add size, weight, and complexity and in some situations where these parameters are strictly controlled (space missions, oil bore holes, nuclear power plants, engine monitoring) are simply not practical to use. Proper radiation shielding is also problematic as it adds size and significant weight to the overall system. By employing field emission devices, particularly with CNT emitters and high temperature compatible materials, complex temperature control and shielding would not be necessary. While this research does not aim to try and exceed the performance of modern FETs, there clearly exist applications in harsh environments where these CNT field emission devices can outperform their semiconductor counterparts.

6.2 Device Design, Fabrication, and Geometry

The basic device concept is shown in Figure 16. The electrodes take on a triode configuration with a cathode, anode, and a gate. A triode functions much like a transistor in that it has the ability to amplify. To operate the field emission triode as a normally “off” device, a voltage is applied between the anode and cathode just below the emission threshold. Once emission begins, a voltage applied to the gate
modulates the emission current between the anode and cathode. Due to the inherent exponential relationship between emission current and applied electric field (Equation 7), a small variance in the gate potential can result in very large changes in the emission current, resulting in amplification.

Figure 16: Schematic representation of the CNT field emitter device concept. (Left) Top-down view showing anode, cathode, gates, and CNTs. (Right) Cross-section of device showing anode, cathode, and CNTs with the gates omitted for clarity.

The basic design concept of a three terminal device has a wide range of possible applications. This type of device is a fundamental component in both digital and analog electronics. When used in analog applications, this device operates as a high-gain amplifier since a small variation in the gate potential can result in large changes in the source-drain current. This is due to the exponential dependence of the emission current with respect to the local electric field at the CNT tips. When used in digital electronics, this device has an inherently high on-off ratio, again due to the sudden onset of the emission current resulting from its exponential dependence on the electric fields. Lastly, the device is capable of having an extremely low gate-source or gate-drain leakage since the electrode arrangement minimizes any unwanted field emission.
In the proposed device, all of the metallic device elements (anode, cathode, and gates all shown in yellow) will be patterned using standard UV lithography. The CNTs shown attached to the cathode in Figure 16 can be deposited using two separate methods: dielectrophoresis (DEP) [71, 74, 75, 132, 133] or thermal chemical vapor deposition (TCVD) [46, 52, 79, 131, 134, 135]. Dielectrophoresis is a physical deposition technique where CNTs are assembled at the desired locations using electric fields, while thermal CVD grows the CNTs in-situ. Though each approach will have a unique fabrication process, the underlying device concept remains the same. The different fabrication processes and results will be described in subsequent sections.

The overall device concept also features a planar geometry which allows for straightforward integration into large scale integrated circuits (ICs). Since the device electrodes are fabricated using conventional semiconductor processing, an arbitrary number of devices can be fabricated in parallel on the same substrate with the only limitation being lithographic tolerances. To add to its integrability, both CNT deposition processes, whether dielectrophoresis or CVD, allow for parallel processing. In the case of thermal CVD, where the CNTs are actually grown in-situ, processing is limited to the size of the reactor in which the CNTs are grown. In the case of dielectrophoresis, the CNTs are deposited across the entire substrate simply
by making the proper electrical connections. Both methods offer a scalable approach to device fabrication.

The device geometry also offers the potential to reduce or possibly eliminate a major source of emitter degradation in addition to relaxing device packaging requirements. Typical of all field emission devices is the degradation of the emission sites due to ion bombardment. These positive ions are created in the vacuum gap by collisions between the field emitted electrons and few gas molecules present within the gap (Figure 17).

![Figure 17: Schematic representation showing the creation of positive ions in the vacuum gap of a field emission triode. Once ionized, the molecule is accelerated towards the cathode and causes damage upon impact resulting in emitter degradation and potential device failure.](image)

Since field emission inherently requires an electric field, ions produced in the anode-cathode gap from electron impacts will experience an acceleration towards the cathode. Although very robust, CNTs are not immune to ion bombardment, and a high flux of incident ions will result in emitter degradation and decreased lifetimes. Although ion impacts present a significant technical hurdle, the problem can be
avoided if the vacuum gap is made smaller than the electron mean free path. With such a small anode-cathode gap collisions with gas molecules will be rare, thus minimizing the chances of a possible ionization event. Calculations have shown that if a molecular diameter of ~0.3 nm is assumed (oxygen molecule) then the mean free path at 1 atm and 300 K is approximately 100 nm using the following relation.

\[ \lambda = \frac{RT}{\sqrt{2\pi d^2 N_A P}} \]  

_Equation 18_

Here, \( \lambda \) is the mean free path in [m], \( R \) is the gas constant in [J/K/mol], \( T \) is the temperature in [K], \( d \) is the atomic (or molecular) diameter in [m], \( N_A \) is Avogadro’s number in [particles/mol], and \( P \) is the pressure in [atm]. An anode-cathode gap of 100 nm is somewhat unreasonable using optical lithography, but may be more suited to electron beam lithography. Having a device that operates at atmospheric pressure [6] would be ideal, but this requires advanced optical or electron beam lithography, so it is more likely the device will be vacuum packaged. If the calculation is repeated with the same parameters but the pressure is reduced to 0.1 atm (~76 torr) a mean free path of ~1.0 \( \mu \)m is obtained. This vacuum requirement is modest compared to other devices requiring vacuum far below 1.0 torr, and should not present a major technical hurdle in the overall packaging of the device.

Reducing the vacuum gap also directly results in lower operating voltages for the field emission device. Since the applied voltage relates directly to the electron
energy, lower operating voltages ensures lower electron energies. If the electron energy is less than the first ionization potential of the gases present in the vacuum gap then even if a collision were to occur, the electron would have insufficient energy to cause ionization.
7 Dielectrophoretic Based Devices

To create a high temperature / high radiation field emission device based on carbon nanotube emitters the most important consideration is the emitters themselves. As discussed earlier, one of the primary hurdles to integrating carbon nanotubes in modern electronic devices is the inability to assemble carbon nanotubes at specific locations. Current techniques are available to do this on a nanotube-to-nanotube basis; however, these solutions (AFM pick-and-place techniques coupled with electron beam lithography) do not represent a viable option for the future due to a lack of scalability. In order for carbon nanotubes to reach their full potential as an electronic material, two elements will be needed: (1) a scalable technique to assemble carbon nanotubes at specific locations, and (2), a method for separating or synthesizing carbon nanotubes with the same chirality and diameter, and hence electronic structure. At present, no technique addressing both issues exists, yet certain techniques do partially meet the stringent requirements and show promise for the future.

For this research, the goal is to create a field emission device based on carbon nanotube emitters, thus control over the emitter location and geometry will be critical. To fabricate such a device, two techniques were chosen to be combined with standard semiconductor processing methods. The two approaches are dielectrophoretic assembly and thermal chemical vapor deposition of carbon
nanotubes. The two techniques, while vastly different in their approach to nanotube assembly, both give rise to a geometrically unique but functionally similar field emission device while also presenting distinct processing differences. These issues, along with the fabrication processes and results unique to each device will be discussed in the following sections.

7.1 Device Concept

One of the most widely used techniques to assemble carbon nanotubes into various configurations is dielectrophoresis. This technique, discussed in Section 5, relies on the interaction of matter with electric fields. Due to the relative dielectric properties of the carbon nanotubes and the suspending medium, it is possible to use electric fields to align, attract, and ultimately assemble nanotubes at specific locations, usually between metallic electrodes [19, 71-73, 75, 76, 133, 136]. Utilizing this phenomena, a device concept was developed that could use dielectrophoresis to create a carbon nanotube emitter array from carbon nanotubes suspended in a dielectric liquid, in this case, dimethylformamide (DMF), chosen for its high dielectric constant of ~38. The dielectrophoretically assembled device concept is similar to Figure 16; however, the first device design iteration for the DEP based devices is shown in Figure 18.
This schematic illustrates the initial DEP device design. Present are three electrically isolated electrodes – anode, cathode, and gate(s) – forming a triode. The triangular shape of the cathode is also intentional. By performing dielectrophoresis between a pointed cathode and a flat anode, the carbon nanotubes are preferentially attracted to the cathode due to the enhanced fields near the tip. This result is especially useful since ideally, only carbon nanotubes attached to the cathode are desirable for functional field emission devices. In practice, as will be shown, the cathode does attract more carbon nanotubes; however, the field enhancement due to the pointed cathode is not enough to completely dominate the dielectrophoresis. As a result, a substantial amount of carbon nanotubes are deposited along the anode as well, which eventually results in a nanotube network bridging the anode-cathode gap.

Dimensions of the device vary, but can be summarized easily. Anode to cathode distances range from 2-10 μm and gate to anode separation is fixed at either 3 μm or 6 μm. Gate to gate distances were also varied from 8, 12, or 16 μm with a gate width of 6 μm.
Before beginning the actual device fabrication, a series of tests were conducted to determine the optimal deposition parameters to use during the dielectrophoresis. Since the physics of carbon nanotube dielectrophoresis, captured in Equation 13, relies partly on the applied electric fields and the corresponding angular frequency, experimental optimization was necessary before device fabrication could proceed.

7.2 Dielectrophoresis Optimization

7.2.1 Angular Frequency

The first parameter to be optimized was the angular frequency of the applied electric field. To optimize this quantity, a sample having long parallel electrodes approximately 2 μm apart (Figure 19) was used in place of the geometry shown in Figure 21. The reason for utilizing a different electrode geometry was to remove any possible effects the pointed cathode may have on the deposition; however, other than the differing electrode geometry, the two substrates were identical. After examining the literature, it was found that a wide range of frequencies can be used to deposit carbon nanotubes. The optimal frequency is often determined by a number of factors including the type and geometry of the carbon nanotubes, the properties of the suspending medium, and the substrates being used. The suggested frequency range found in the literature typically ranged from 100 kHz to 30 MHz, thus the frequency values of 30 MHz, 10 MHz, 500 kHz, and 100 kHz were arbitrarily chosen [71-76, 124, 132, 133, 136-139].
To perform the deposition process, the substrate, typically a 1 cm$^2$ die, is placed into a small glass dish and electrical connections were made. Once electrical contact was established, a small amount of the carbon nanotube suspension was placed onto the substrate surface making sure the entire surface of the die was covered. The concentration of the suspension was 0.5 μg/mL. Details on the preparation of the carbon nanotube suspension can be found in Section 5.3. Once the suspension was in place, sinusoidal voltages at 30 MHz, 10MHz, 500 kHz, and 100 kHz were applied to each set of electrodes using a function generator. The voltage amplitude was constant at 10 V for this particular experiment and applied to each set of electrodes for 15 seconds. It should be noted that the optimization of the angular frequency was also attempted at other voltages; however, the early data was inconclusive resulting from the voltages being insufficient or too large for the given electrode geometry. Despite being inconclusive, those initial results did provide an excellent starting point for determining the optimal electric field strength. Furthermore, the alignment and uniformity of the carbon nanotube networks formed using a parallel electrode configuration would later lead to an important modification to the overall device geometry.
Following the completion of the deposition, each substrate was rinsed in isopropanol and dried in argon. The results of the experiment are summarized in the SEM images shown in Figure 19. Here the frequencies of 30 MHz, 10 MHz, 500 kHz, and 100 kHz correspond to Figure 19A, Figure 19B, Figure 19C, and Figure 19D respectively. Since the overall goal is to use the deposited nanotube network as a field emitter array, a reasonably dense, uniform array is most desirable. The results indicate that the optimal frequency based solely on the SEM image analysis is 500 kHz. Increasing the frequency from 500 kHz to 10 MHz seems to have a negative affect on the deposition process as fewer nanotubes attach to the electrodes. Further increasing the frequency exacerbates the problem as even fewer nanotubes are
attaching at 30 MHz. Since the nanotubes used were all single-walled, statistically, two-thirds of them were semiconducting while the remaining third were metallic. In accordance with Figure 14, increasing the deposition frequency repels the semiconducting nanotubes from the electrodes rather than attracting them, which explains the observed behavior. Decreasing the frequency appears acceptable down to 100 kHz; however, it is clear that a frequency of 500 kHz produces the most desirable nanotube arrays.

7.2.2 Electric Field Strength and Deposition Time

Though the purpose of the dielectrophoresis done on the substrates with parallel electrodes was solely to optimize the angular frequency, it did elucidate a basic understanding of the electric field strength needed to perform the deposition in a timely manner. From the results shown in Figure 19, it would appear that an electric field of ~3.5 V/μm applied for 15 seconds produces an excellent carbon nanotube network (Figure 19C). The electric field here is calculated by taking the root-mean-square (RMS) voltage, 7.07 V, and dividing it by the electrode separation of approximately 2 μm.

Using this data, the device substrates containing the pointed cathodes could be used to optimize the electric field strength and deposition time needed to produce nanotube networks similar to Figure 19C. The parallel electrodes were not used for this series of tests simply because they lacked an electrode with a triangular geometry. From earlier discussions it is known that the triangular structure will
increase the electric field near its tip apex, which results in a stronger
dielectrophoretic force on the carbon nanotubes. As a result, data obtained from the
parallel electrodes would not be fully applicable to the device geometry, thus
separate tests had to be performed.

For this series of tests, substrates with a nominal anode to cathode gap of 4 μm were
chosen. The carbon nanotube suspension concentration was 0.5 μg/mL and the
frequency of the applied voltage was 500 kHz. A voltage amplitude of 10 V was then
applied to each device for times of 5, 10, 15, 30, 45, and 60 seconds. Following the
deposition, the substrates were rinsed in isopropanol, dried in argon, and examined
via SEM. The SEM images showing the results are given in Figure 20.

Calculating the electric field strength in the same manner as before, a value of ~1.75
V/μm is obtained. The SEM images of Figure 20A-F correspond to deposition times
of 5, 10, 15, 30, 45, and 60 seconds respectively. The SEM images show that
deposition times less than 15 seconds will not produce a sufficient nanotube network
for the desired emitter structure (Figure 20A and Figure 20B). As the time increases
from 15 seconds to 30 seconds (Figure 20C and Figure 20D), the nanotube network
becomes ideal for an emitter structure; however, a deposition longer than 30 seconds
leads to the formation of large clumps of nanotubes between the anode and cathode
(Figure 20E and Figure 20F). Measurements of these structures showed them to be
significantly thicker than the metal electrodes and could often be more than a micron
in height. Naturally, these large structures are not desirable since they would likely form poor emitters, and thus should be avoided. In some cases, these structures form even at short deposition times, mainly due to the presence of very large nanotubes bundles not dispersed during the sonication. This issue can be reduced by improving the sonication and performing a filtration step to remove as many of these bundles as possible.

Figure 20: SEM images showing DEP results for single walled carbon nanotubes deposited between a pointed cathode and a flat anode. The anode to cathode gap is nominally 4 \( \mu \text{m} \). The deposition times were (A) 5 seconds, (B) 10 seconds, (C) 15 seconds, (D) 30 seconds, (E) 45 seconds, and (F) 60 seconds. The voltage amplitude and suspension concentration were held constant at 10 V and 0.5 \( \mu \text{g/mL} \).

The results from the optimization of the electric field strength and deposition time do not necessarily point to an exact set of process parameters. Rather, the results suggest that there is a range of acceptable electric fields and deposition times that can produce carbon nanotube networks like those shown in Figure 19C and Figure 20D.
It does appear that electric fields greater than \( \sim 1.5 \text{ V/\mu m} \) can rapidly produce desirable nanotube networks in short periods of time, typically 30 seconds or less. However, it is certainly possible to perform dielectrophoresis successfully at lower electric fields, provided that the deposition time increases appropriately. As long as the dielectrophoretic force exerted on the nanotubes is significantly greater than the combined action of thermal fluctuations and flow within the suspension, the nanotubes will be attracted to the electrodes. This result will prove useful in subsequent device geometry iterations.

### 7.3 First Generation Device Fabrication

With the dielectrophoresis optimization completed, the fabrication of the device could proceed with the first fabrication step being standard UV photolithography to generate the electrode pattern on the substrate. Here, the substrate is a thermally (wet) oxidized \(<100>\) silicon wafer where the oxide ranges from 0.5 to 1.5 \(\mu\text{m}\). Since the metal deposition is performed by electron beam evaporation, a highly directional deposition method, a negative photoresist (Futurrex NR1-3000 PY) is preferred due to the inverted sidewalls left after exposure and developing as shown later in Figure 38. To form the anode, cathode, and gates, a combination of Cr and Au is evaporated. The Cr is first deposited to a thickness of 30-50 nm, and serves as an adhesion layer for the Au. Once the Cr is deposited the Au is evaporated, without breaking vacuum, to a thickness of 100 nm. Following the metal deposition, the substrate is soaked in warm acetone to dissolve the photoresist and lift-off the
unwanted metal. The resulting device geometry is illustrated in Figure 21, corresponding to the die layout shown in Figure 22.

The layout shown in Figure 22 shows a single die after it has been diced from the larger silicon substrate. The initial design produced 5 mm by 5 mm die, each containing 5 identical, electrically isolated devices. Each device consisted of three electrodes; an anode, cathode, and two gates. For clarity, any closed polygon shown in Figure 23 will become the metallic conductors once the lithography shown in Figure 21 is complete.
With the DEP parameters for single walled CNTs optimized, the dielectrophoretic deposition can be completed. To perform the dielectrophoresis, the die was placed into a shallow dish, electrical contact made to the device, and a suspension consisting of single walled nanotubes pipetted such that the surface is entirely covered. The suspension concentration used was 0.5 μg/mL and was prepared in accordance with the procedure outlined in Section 5.3. A sinusoidal voltage with an amplitude of 10 V and a frequency of 500 kHz is then applied to each device for 30 seconds using a function generator (Stanford Research Systems DS340) to form the carbon nanotube networks between the anode and cathode. Once the deposition was completed on each device, the die was removed from the suspension, rinsed in isopropanol, and dried with argon. While most die progressed to the next fabrication step, a few were selected for SEM analysis to verify a successful deposition. Typical results of this fabrication step are shown in Figure 24.

Figure 24: SEM image showing a single device immediately after single-walled carbon nanotube deposition by DEP. The sample shown has a 4 μm anode to cathode gap.
As the SEM image shows, a dense carbon nanotube network has deposited between the anode and cathode; however, the nanotube network also creates electrical shorts between all of the electrodes. In order for the device to function properly, conductive paths must be removed. Thus, to remove the unwanted nanotubes, a second lithographic step is performed. In this step, a rectangular masking layer, typically photoresist or metal, is patterned on top of the cathode and extended out towards the anode to cover some of the nanotubes in the gap. This is illustrated in the SEM images of Figure 25.

![Figure 25: (A) SEM image showing the masking layer to protect and define the carbon nanotube emitter structure before the unwanted nanotubes are removed. (B) SEM image of the carbon nanotube emitter structure after the unwanted nanotubes and masking layer are removed.](image)

As the SEM image in Figure 25A shows, the masking layer is positioned such that it covers a stripe of the deposited nanotube network while leaving the remaining sections accessible to further processing. With the nanotubes that will eventually form the emitter structure protected, the unwanted nanotubes can be removed by an oxygen plasma in a reactive ion etching (RIE) system (Trion Phantom III RIE/ICP). This particular plasma directly attacks the carbon nanotubes and removes them from
the substrate. The process is performed at a pressure of 30 mtorr, oxygen flow rate of 50 sccm, and RIE power of 100 W. The results of the reactive ion etching are shown in Figure 25B. Here, a chromium mask was used to protect the carbon nanotubes from the oxygen plasma. The nanotubes that were beneath the chromium mask remain intact, while the exposed nanotubes were etched away. In addition to etching the unwanted nanotubes, the oxygen plasma removes organic contaminants on the substrate surface and readies it for further processing.

The next step in the fabrication process involved the cantilevering of the carbon nanotubes such that the tips would protrude slightly outward as shown in Figure 18. This step is very important for two reasons. By producing a cantilevered emitter structure the electric fields at the nanotube tips will be enhanced more than if the nanotubes were simply lying flat on the oxide. This has a direct impact on the operating voltages of the devices, which become more desirable the lower they are. Additionally, by placing the emitting tips out in the vacuum gap, the detrimental effects of charging the underlying oxide could be reduced. It is not unreasonable to expect a field emitting nanotube lying on the oxide surface would not only require higher electric fields, but would also inevitably charge the surrounding oxide, further hindering emission.

Before using samples containing processed carbon nanotubes, the cantilevering etching procedure was carried out on samples having only the original anode,
triangular cathode, and gate electrodes. No nanotubes were present on these substrates. These samples were subjected to numerous etchants including a buffered oxide etchant (J. T. Baker), dilute hydrofluoric acid (J. T. Baker), and hydrofluoric acid vapor phase etching. In each case, various concentrations and etch durations were attempted with the goal of removing a small amount of the underlying oxide on the order of 50 to 100 nm. The results of these preliminary experiments are summarized by Figure 26.

![Figure 26: SEM images showing the metallic cathode point cantilevered after being etched in a buffered oxide etchant (BOE).](image)

The initial results on test samples appeared promising with the pointed cathode undercut a distance of a few hundred nanometers. Given these results, the etching was attempted on samples with a patterned carbon nanotube network using buffered oxide etch (BOE). The test samples came in two types: samples where the protective masking layer over the CNTs had been removed (using acetone if the mask was photoresist, or the appropriate metal etch if the mask was metallic) or samples where the metal masking layer remained intact. Photoresist protective layers were always removed since it was not desirable to have a non-conductive material contacting the
nanotubes. For the samples without the protective masking layer a very short etch in BOE was performed in an effort to remove a small amount of oxide from beneath the carbon nanotubes. For the samples with the metallic protective layer intact, a slightly different approach was taken. It was hypothesized that since the nanotube network was very thin compared to its width, a cantilevered structure may not be rigid enough, and as a result, would bend significantly towards the oxide surface. To preempt this potential problem, the metal protective layer would also serve as a structural support for the nanotube network. In addition, it would also provide an improved electrical contact to the nanotube network during the testing phase. In this instance, a BOE etch to remove the oxide beneath the metal/nanotube structure was done followed by a short metal etch to expose the tips of the nanotubes. An illustration of the substrate before and after the etching is shown in Figure 27. Once the etching was completed, electrical tests were performed to verify if field emission could be achieved.

Figure 27: (A) Schematic showing carbon nanotubes encapsulated within the protective metal layer prior to etching. (B) Schematic showing the exposed carbon nanotube tips resulting from etching both the protective metal layer and the underlying silicon dioxide.
7.4 Preliminary Electrical Tests

With the fabrication completed, electrical testing could begin on the devices with the electrical test setup illustrated in Figure 28.

![Figure 28: Electrical setup used for preliminary field emission testing. Shown are the anode, cathode, gates, and voltage source-measure unit (SMU).](image)

Both the cathode and gates are shorted together and wired to ground while the anode is wired to the positive pole. The entire device is placed within a vacuum chamber and brought to a pressure of $10^{-6}$ torr. To initiate field emission, the anode voltage was slowly increased while simultaneously measuring the current using a Keithley 237 High Voltage Source-Measure Unit. The results would show that none of the samples exhibited electrical behavior characteristic of field emission. Instead, many of the samples were destroyed as a result of an electrical breakdown between the anode and cathode. In each instance, the anode voltages had reached very high levels resulting in electric fields well above 10 V/μm. SEM images of devices that experienced electrical breakdown are shown in Figure 29.
From the images, it is apparent that significant damage has been caused to the electrodes as a result of the breakdown. There is clearly a damaged region on both anodes where some metal is missing, and the cathodes show signs of cracking. Figure 29A illustrates a device where the protective metal layer was not removed while Figure 29B shows a device where the protective metal layer has been etched away. In both cases, the presence of the metallic protective layer made little difference as the results of the electrical testing for both devices were essentially the same. Additionally, field emission from carbon nanotubes should occur at electric fields well below 10-15 V/µm (typically at 1-3 V/µm for a robust device) thus large electric fields are an indication that modifications to the device fabrication process or geometry are needed.

Despite failing to produce field emission, the results obtained from these devices initiated a set of fabrication and geometrical modifications in an attempt to produce
an operable device. Throughout the fabrication, numerous difficulties were encountered despite producing testable devices. With the results from the initial electrical tests, it was concluded that numerous issues needed to be addressed to improve the likelihood a device would operate properly once fabrication was completed.

### 7.5 First Generation Fabrication Process Analysis

#### 7.5.1 From Serial to Scalable

Given the initial results obtained from the 1st generation DEP devices, it was concluded that modifications to the geometry and fabrication process were necessary to produce working devices. For the 1st generation devices, the process adopted a serial approach to the DEP deposition. With each die containing five electrically isolated devices, the DEP deposition process had to be performed five separate times per die. Scaling such a process to a wafer with hundreds of such die would be extremely tedious given the serial nature of the deposition. Having to perform the nanotube deposition numerous times, even under the same experimental conditions, increases the likelihood of uniformity and reproducibility issues. It was far more desirable to devise a method where all the devices could undergo the DEP process simultaneously. This issue was resolved simply by redesigning the electrode layout such that, at the wafer level, all the anodes were wired together and all the cathodes were wired together. In this configuration, two electrical contacts could be made to
an entire wafer and the deposition completed on all devices in parallel. The resulting change to the device layout is depicted in Figure 30.

![Figure 30: (Left) Die level DEP device layout compared to (Right) wafer level DEP layout. The die level process will require multiple depositions since the devices are electrically isolated while the wafer level process will require only a single deposition because the devices are wired in parallel.](image)

In the die level layout, each DEP step produces a single viable device. In the case of a wafer level layout, a single DEP step produces a wafer of viable devices. The benefits here are obvious as parallel fabrication methods are more efficient and reduce the possibility for device-to-device variance.

### 7.5.2 Uniformity and Reproducibility

Though carbon nanotube depositions were successful on 1st generation samples, they often lacked the reproducibility to be considered a reliable process. In most instances, the deposition produced an ideal carbon nanotube network; however, a significant fraction of the depositions resulted in undesirable morphologies. In some cases, very few carbon nanotubes were deposited between the anode and cathode,
while in other cases, too many, despite identical experimental conditions. The most common issue was a massive agglomeration of carbon nanotube bundles forming a tall, mound-like structure in the active region of the device that was significantly thicker and denser than the optimal nanotube network. Examples of such structures are shown in Figure 31. Though plasma etching by RIE could remove this material, it would be at the expense of other devices on the die unless a separate, albeit extremely impractical, masking step was performed.

![Figure 31: SEM images showing examples of the tall, mound-like structures formed in the active region of the device during the DEP deposition process.](image)

### 7.5.3 DEP Electrode Geometry and Separation

Upon reviewing recent DEP experiments, a comparison was made between the carbon nanotube networks assembled between parallel electrodes (test structures, 2 μm gap) and networks assembled between a pointed cathode and a flat anode (1st generation geometry, 4 μm gap). Upon viewing the SEM images of each sample type, it was observed that the parallel electrode geometry produced excellent carbon nanotube networks that persisted over relatively long distances, typically on the
order of millimeters. This was in stark contrast to the pointed samples that showed
device-to-device variability over the same length scales, even when the devices were
wired in parallel and deposition occurred simultaneously. This realization prompted
a set of experiments on some pre-fabricated test samples having parallel sets of
electrodes with larger gap separations on the order of ~20 μm. The DEP was
performed using a function generator at a voltage amplitude of 10 V with a
frequency of 500 kHz. The carbon nanotube suspension, containing only single-
walled carbon nanotubes, was at a concentration of 10 μg/mL. Various deposition
times were used, typically on the order of a few minutes. SEM images showing the
results of these tests are shown in Figure 32.

![SEM images of carbon nanotubes deposited between a set of parallel
electrodes separated by 20 μm. The resulting nanotube network is very dense
and uniform over relatively long distances.](image)

Visual inspection of the SEM images of the DEP confirms that the parallel electrode
groupy produces significantly more uniform networks than the pointed samples.
Although the SEM images conclusively show the benefits of incorporating a parallel
electrode geometry rather than pointed samples, the relationship between the
electrode geometry and spacing remained unclear and warranted a more in-depth study.

From the SEM data it was determined that the electrode dimensions play an important role in the CNT network deposition reproducibility over macroscopic distances. For single-walled carbon nanotubes at a suspension density of 10 μg/mL, there is on average one single-walled carbon nanotube per μm³ of suspension. For small, closely spaced electrodes for which the electric field gradients are significant within only a few μm³, it is not surprising that networks formed between different pairs of electrodes across macroscopic distances are dissimilar. However, with larger electrodes (both size and separation), where the electric fields interact with a volume >10⁴ μm³, the similarity among devices is much better because random variations in local CNT density in the suspension are averaged. Thus, electrode geometries are chosen such that the interaction volume is of order 10⁴ μm³. These initial results point to what may be a limit in practical DEP assembly of CNTs. At a density in suspension of 10 μg/ml, there is some agglomeration of CNTs into bundles, which reduces the suspension uniformity (most studies use densities within this range [71, 73, 75, 76, 138]). To mitigate this problem, the CNT suspensions are horn sonicated and subsequently filtered to remove any remaining large bundles. However, unless the CNT density in the suspension can be increased significantly without a concomitant increase in CNT agglomeration, wafer-scale fabrication of CNT devices
may be limited to those devices where the electrodes interact with a sufficiently large volume of suspension

Using newly designed photomasks for the 2nd generation DEP devices a series of tests were conducted to examine the relationship between electrode geometry and separation distance and to elucidate more details on the physics and evolution of the deposition process. The DEP process was performed using lithographically-patterned electrodes (50 Å Cr adhesion layer and 1000 Å Au) on 100 mm glass wafers or thermally oxidized Si substrates, each having 432 parallel DEP sites. As in previous depositions, the substrates were placed into a shallow dish, electrical contact was made, and 10 mL of CNT suspension at a concentration of 10 μg/mL were pipetted to cover the surface. Deposition times ranged from 5 seconds to 15 minutes with a sinusoidal peak-to-peak voltage of 24 V at a frequency of 100 kHz. The driving voltage was supplied by a PA-96CE linear amplifier (Apex Precision Power / Cirrus Logic).

A note should be made here about the changes in DEP parameters that had been used in past processes. Previous nanotube depositions were almost exclusively conducted on single devices or a small number of samples wired in parallel. Since the contact resistance between the CNTs and the metal electrodes was large, the voltage source did not need to provide a large current to maintain the output voltage amplitude. Thus, it was possible to use a function generator so long as its power limits were not
exceeded. As a result of wiring many devices in parallel, such as was done for the 2nd generation devices, the function generator was no longer able to meet the power requirements for the DEP process. Thus, an amplifier capable of maintaining sinusoidal voltage amplitudes of 10-12 V at frequencies of 100-500 kHz and drive currents on the order of 10-50 mA was required. Changes were also made to the voltage amplitude, suspension concentration, and deposition time. Since the amplifier could not reliably achieve voltage amplitudes larger than 12 V (larger was possible, but not stable), the electric fields generated during the DEP would be lower (compared to previous depositions) due to larger electrode spacing. To compensate, the suspension density and deposition time were increased to improve deposition uniformity and reproducibility.

Table 3: Comparison between CNT DEP processes using single or a few devices wired in parallel and large scale wafer-level depositions on many devices wired in parallel.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Small-Scale Deposition (single / few devices)</th>
<th>Wafer-Level Parallel Deposition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Amplitude</td>
<td>10 V</td>
<td>12 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>500 kHz</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Suspension Concentration</td>
<td>0.5 μg/mL</td>
<td>10 μg/mL</td>
</tr>
<tr>
<td>Type of Nanotubes</td>
<td>SWNT</td>
<td>SWNT</td>
</tr>
<tr>
<td>Deposition Time</td>
<td>&lt; 1 minute</td>
<td>15 minutes</td>
</tr>
</tbody>
</table>

A PA-96CE linear amplifier (Apex Precision Power / Cirrus Logic) satisfied these requirements, though it was not able to maintain a stable 500 kHz signal throughout the entire deposition process. As a result, the deposition frequency was changed to 100 kHz, which would also give similar results evidenced by previous work shown
in Figure 19D. A summary of the small-scale and wafer level DEP parameters is given in Table 3.

7.5.4 Evolution of Carbon Nanotube Dielectrophoresis

DEP was performed at fixed sinusoidal voltage amplitude of 12 V supplied by a PA-96CE amplifier. A series of DEP experiments were done, each for a different deposition time, to produce the chronological images shown in Figure 33. For each DEP deposition process a new substrate was used. A single substrate cannot be used repeatedly since the repeated rinsing, drying, and imaging would substantially affect the deposition, and hence alter the results. Following completion of the DEP process, the substrates were rinsed in isopropanol, dried with argon, and inspected by SEM. In some experiments, DEP was performed while the apparatus was in an ultrasonic bath. The CNT networks produced by DEP showed similar CNT density, coverage, and alignment on randomly selected sites over the entire 100 mm substrate. The uniformity of the deposition was also assessed using SEM images. At each selected location, the uniformity and coverage of the deposited CNT network appeared similar, thus demonstrating consistent reproducibility across the substrate.

Figure 33B and Figure 33C illustrate the early phases of CNT DEP where the CNTs distributed themselves along the metal electrode and did not extend significantly beyond their own length into the gap. It is instructive to compare this result with metallic nanoparticle (NP) [140] and nanowire (NW) [141] DEP. NPs and NWs tend to form chains, rather than assembling in a row at the edge of the electrode. We
hypothesize that the induced dipole moment of the NPs/NWs is larger, due to their larger size; and when the NPs/NWs are attracted to the electrode edge the electrical impedance between the electrode and metallic NP/NW is smaller. Therefore, the point of maximum field gradient moves immediately to a newly-attracted NP/NW, causing any subsequent NP/NW to be attracted there. This process continues and chains of NPs/NWs form. In contrast, CNTs appear to have a smaller induced dipole moment and larger electrode-CNT impedance under similar conditions, and therefore it takes a denser collection of them along the electrode edge to shift the point of maximum field gradient to the tips of the CNTs.

![Figure 33: SEM images showing the chronological evolution of the dielectrophoretic deposition of single-walled carbon nanotubes.](image)

Figure 33D and Figure 33E show that after the first row of CNTs assembled at the electrode edges, there was a subsequent chaining of CNTs to bridge the gap. This suggests that, during DEP, the CNT-CNT coupling was strong, allowing linked
CNTs to have an induced dipole moment similar to a single long CNT. This allowed the electric field gradient maximum to shift to the advancing tip of the chain, and continue its growth until it bridged the gap.

Figure 34: (A) SWNT DEP after 20 seconds showing CNTs evenly spaced and aligned perpendicular to the electrode edge. (B) SWNT DEP after 40 seconds showing subsequently deposited CNTs becoming less aligned due to changes in the local electric fields.

This hypothesis predicts that the initially deposited CNTs at any location should be more aligned than CNTs deposited at later times. At early times, the fields responsible for attracting and assembling the CNT network have not been substantially modified by CNT deposition so they remain perpendicular to the electrode edge. As the density of the CNTs at the electrode edge increases, the local electric fields are modified, such that one would expect subsequent CNTs not to deposit perpendicular to the electrode edge. Figure 34 demonstrates this effect. After a 20 sec. experiment, the CNTs were primarily perpendicular to the electrode edge (Figure 34A). After a 40 sec. experiment, it is clear the subsequent CNTs deposited near the edge had varying orientations, while those farther from the electrode edge were aligned (Figure 34B).
During the deposition process, the root-mean-square (RMS) current amplitude and its relative phase were measured in Figure 35. The observed behavior was reproducible from one deposition to the next. Figure 33 and Figure 35 together demonstrate that the current measurement is an effective probe of the density of the assembled CNT networks.

![Figure 35: Plot of the in phase and out of phase components of the RMS DEP current as measured during the deposition process.](image)

Initially, the out of phase component, which is linearly related to the capacitance in a simple circuit model of a resistor and capacitor in parallel, rose quickly and reached a transition point, at approximately $t = 1$ minute, where the slope changed. Comparing the plot in Figure 35 to the SEM images in Figure 33, this slope change occurred as the CNTs began to bridge the electrode gap. Qualitatively, the fact that there are different slopes on either side of this transition is not surprising. Initially,
the CNTs were expanding into the gap and bringing the two electrodes closer together. Once the bridging had begun, the primary effect of further CNT deposition was to fill in gaps in the network. Quantitatively, the values for the two slopes are difficult to predict, as they depend on details of the electronic interactions between the CNTs in suspension which are not well known. One might apply a similar argument to the slope of the resistance of the network (linearly related to the in-phase component of the current).

![Figure 36: Current as a function of time for sonicated vs. non-sonicated DEP processes. The sonicated sample required more than twice the deposition time to reach comparable current amplitudes. (A) Corresponds to a non-sonicated sample for $t = 5$ minutes. SEM results are shown in Figure 37A. (B) Corresponds to a sonicated sample for $t = 10$ minutes. SEM results are shown in Figure 37B.](image)

However, the suspension itself had a resistance of about 3 kΩ, and any CNT bridges that formed were in parallel with this resistance. Since it is likely that any individual CNT bridge had a very large resistance in comparison to the suspension, a very
gradual change in slope is expected. This is because it takes many CNT bridges in parallel in order to significantly reduce the total resistance below that of the suspension alone.

DEP was also performed in the presence of sonic energy generated by a laboratory ultrasonic cleaning bath. The results indicate a marked increase, of about a factor of two, in deposition time in order to achieve the same current amplitude (Figure 36). SEM images confirm that the network densities were very similar for similar final current amplitudes (Figure 37). Since the current through the entire DEP network is linked to the CNT network density and thickness at the deposition sites, it can be assumed that by applying additional energy, it becomes more difficult for CNTs to form electrical contacts with neighboring CNTs or to the metal surface. As a result, the assembly rate for the CNT network decreased. This also suggests that there may be ways to improve CNT alignment. For example, if sonication reduces the CNT-CNT interaction, following the observations described above one would expect to be able to assemble a greater density of CNTs perpendicular to the electrode edges before they start depositing with other orientations.
7.6 Second Generation Device Fabrication

After analyzing the first generation device fabrication process a few major modifications were made. The most significant of which were the changes to the DEP process, while the other step involved an improved etch to cantilever the CNT emitters. With these modifications, a new fabrication process was developed to accommodate these changes.

7.6.1 Electrode Lithography and Carbon Nanotube Deposition

The fabrication of the 2nd generation DEP-based device begins with standard UV photolithography to generate the electrode pattern on the substrate. Here, the substrate is again a thermally oxidized <100> silicon wafer where the oxide ranges from 0.5 to 1.5 μm. This first lithographic step will form the electrode network necessary to perform dielectrophoresis at the wafer level. Once this step has been completed, portions of this electrode network, after some required etching, will be used as the anode and cathode. As in previous processes, this first metal layer is comprised of 30 to 50 nm of Cr serving as an adhesion layer for the 100 nm of Au.
above it. These metals are deposited via electron beam evaporation, which being a highly directional deposition method, permits the use of a negative photoresist.

The importance of the negative photoresist cannot be underestimated as it gives smoother edges to the deposited metal films. This is critically important when fabricating field emission devices as any sharp asperity can potentially be an emission site. The smoother electrode edges are due to a combination of the directionality of the evaporation process and the inverted sidewalls of the negative photoresist left behind after exposure and developing. An inverted sidewall profile, shown schematically in Figure 38A, causes a physical discontinuity in the deposited metal film, thus permitting the removal of the unwanted metal via lift-off without any tearing or possible delamination. A more typical profile, often seen when employing positive photoresists, is shown schematically in Figure 38B.

Here the sidewall profile is vertical or near-vertical, and while lift-off can be performed, any sloping of the sidewall will result in the deposition of a thin metal
film. In order to complete the patterning, this film would effectively have to be torn during the lift-off step, which can result in jagged edges and delamination of the film in many instances.

Once the metal has been deposited by the e-beam evaporator, the substrate is soaked in warm acetone to dissolve the photoresist and lift off the unwanted metal. The pattern left behind (Figure 39A) will form the electrode network used for the CNT dielectrophoresis.

Following the electrode deposition, the carbon nanotubes were deposited by dielectrophoresis in the manner outlined earlier. The substrate is first placed into a shallow dish, electrical contact is made, and approximately 10 mL of single-walled carbon nanotube suspension is used to cover the entire substrate. Prior to the deposition, the suspension is filtered and sonicated in the usual manner. The concentration of the suspension was approximately 10 μg/mL. With the suspension
covering the entire surface of the substrate, a fixed sinusoidal voltage amplitude of 12 V at a frequency of 100 kHz was applied by a PA-96CE amplifier for 15 minutes. During the deposition process the RMS current was observed in order to monitor the progress of the deposition. Upon completing the 15 minute deposition the substrate is rinsed in isopropanol and dried in argon. An SEM image of a typical, single deposition site is shown in Figure 39B. Here a uniform CNT film is shown to have deposited between the electrodes and is suitable for further processing. To verify uniformity across the wafer, other deposition sites were examined randomly by SEM. The results would show the quality of the CNT deposition exhibited in Figure 39B was consistent across the wafer. Figure 40 illustrates this by showing SEM images of 9 randomly selected sites on the same wafer. From the SEM images it is clear that the CNT DEP process can reproducibly generate uniform CNT networks suitable for use in the desired devices. Moreover, although the depositions were performed for specific times rather than network currents, it should be possible to use current monitoring to assess the quality of the networks as well.
Figure 40: (A-I) SEM images taken at random locations across the wafer illustrating the uniformity and reproducibility of the CNT DEP process at the wafer level. In each image the scale bar corresponds to 50 microns.

7.6.2 Carbon Nanotube Etching and Device Isolation

Once the carbon nanotubes are deposited, a second lithographic step is performed. In this step, each deposition site across the wafer must be electrically isolated from its neighbors. Since the original electrode pattern is used for the DEP process, all of the devices are wired together in parallel. To electrically isolate the devices, a positive photoresist (Shipley 1827 or 1813) is patterned and the Au is removed followed by the Cr using the appropriate metal etchants (Technostrip II). With the metal fully removed from the photoresist vias, some portions of the deposited carbon nanotube
network are exposed. These areas are undesirable and are removed using an oxygen plasma generated by an RIE system. In addition to removing unwanted nanotubes, the RIE will also simultaneously define the eventual CNT emitter structure. The RIE is completed at a base pressure of 30 mtorr, oxygen flow rate of 50 sccm, and an RIE power of 100 W. The duration of the RIE is typically 8-10 minutes depending on the thickness of the deposited nanotube network. The results of these processing steps are shown schematically in Figure 41 and imaged by SEM in Figure 42.

Figure 41: Cross-section and top-down views of the substrate after the second lithographic step. Here, the Au and Cr are first removed via wet etching, followed by an RIE oxygen plasma to remove any undesirable nanotubes. The cross-section is taken along the dashed line shown in the top-down view.
7.6.3 Cathode Deposition and Trench Formation

Upon the completion of the RIE to remove undesirable nanotubes, the photoresist mask is removed by soaking the substrate in warm acetone. After drying in argon, another layer of negative resist is deposited onto the surface. The substrate is placed into an electron beam evaporator and 30 to 50 nm of Cr is deposited, followed by 100 nm of Au. Again, the Cr is solely for adhesion while the Au forms the bulk of the metal conductor. The resulting pattern from the metal deposition is shown schematically in Figure 43 and also in the SEM image of Figure 44.
Figure 43: Cross-section and top-down views of the substrate after the third lithographic step. Here, the Au and Cr are patterned via lift-off to form an electrical contact to the nanotube network while also forming the bond pad for the cathode. The cross-section is taken along the dashed line shown in the top-down view.

Figure 44: SEM image after deposition of the electrical contact / cathode bond pad. The deposited metal will make contact to one end of the CNT network and will extend a few microns along its length.

Compared to Figure 42, the metal deposition is readily apparent in Figure 44. Here the gates are deposited symmetrically about the nanotube emitter structure to maximize effectiveness. The cathode contact/bonding pad electrode is shown to make contact to the edge of the nanotube network closest to the cathode edge. This will help to lower the contact resistance between the nanotubes and the cathode which will help reduce operating voltages.
Upon completing the lift-off to define the cathode and the gates another RIE step is performed. In this step, positive photoresist is spun onto the substrate and a small rectangular window is opened over a portion of the nanotube network and the anode as shown in Figure 45. The purpose of the photoresist is to act as an etch mask for an RIE process. The RIE process will perform two critical tasks; first, the plasma will remove any excess nanotubes, particularly those present along the edge of the anode (Figure 44). The plasma will also etch a small portion of the nanotube network to define the edge of the emitter. The second purpose of the RIE etch is to create a trench in the active region of the device to facilitate more efficient field emission. Previous electrical tests of nanotube networks laying on the dielectric substrate surface did not yield any field emission. The primary hypothesis is the proximity of the dielectric substrate to the nanotube tips significantly reduced the electric field enhancement.

Figure 45: Cross-section and top-down views of the substrate after the fourth and final lithographic step. Here, a small rectangular window is opened above part of the nanotube network and the anode. The photoresist will serve as an etch mask for the RIE process which will remove any excess nanotubes and create the trench in the substrate.
As a result, the voltages applied during the initial tests were very high, and typically caused catastrophic arcs across the device as opposed to well-controlled field emission. It is presumed that even had field emission occurred in these early tests, the dielectric substrate would have experienced some charging due to its proximity to the emitting nanotube tips. To deal with charging, the dielectric substrate in the active region of the device is recessed from the emitters, which is accomplished using an RIE etch process. The etching process occurs at 50 mtorr, with a CF₄ flow rate of 50 sccm, and at an RIE power of 230 W. This particular recipe is used to etch both the dielectric substrate (typically SiO₂) and the nanotubes. Though the nanotubes are not chemically etched by the CF₄ plasma, the ionic bombardment is enough to destroy any exposed nanotubes. The duration of the etch process varied depending upon the desired depth of the trench, typically lasting 5-10 minutes at an etch rate of approximately 50 nm per minute. Following the RIE process, the substrate was soaked in warm acetone to remove the remains of the photoresist etch mask.

### 7.7 Second Generation Fabrication Process Analysis

#### 7.7.1 TiW Sacrificial Layer and Process Integration

Upon SEM imaging of the substrate, it was determined that further modifications were needed in the fabrication process due to the RIE etch process. The result of the RIE is shown in Figure 46. In the image it is clear that even after a prolonged soak in warm acetone, some of the photoresist remains intact on the surface. In an attempt to
remove the photoresist structure, the substrate was treated for 5 minutes in an \( \text{O}_2 \) plasma. The process was completed at a base pressure of 30 mtorr, an \( \text{O}_2 \) flow rate of 50 sccm, and an RIE power of 200 W. This technique is often employed to clean substrates of residual organics as well as ash photoresists.

Figure 46: SEM images showing the results of the RIE etch to remove excess nanotubes and to define a trench in the active region of the device. (Left) SEM image of the as-produced photoresist fence structure along with substantial residual contamination in the form of particulates on the surface. (Right) SEM image of the photoresist fence structure after a 5 minute \( \text{O}_2 \) plasma in the RIE. It should be noted that the images show two different devices; however, the \( \text{O}_2 \) plasma treatment had no effect on the photoresist structure though it did help reduce surface contamination.

Figure 46 (Right) shows the sample after an oxygen plasma. It is clear the plasma had little to no effect on the photoresist fence structure, though it does remove some of the residual particulate contamination on the surface.

A thorough characterization of the “fence” material was not completed (assumed to be primarily photoresist); however, it is believed that the CF\(_4\) etch caused some fluorination of the photoresist, essentially rendering it inert to most compatible
etching methods. Another possibility is that the material is not photoresist but a fluoropolymer film deposited along the sidewalls of the photoresist etch mask.

Despite many attempts, the contamination could not be removed. Since the trench is an essential element to the device, eliminating the RIE step was not an option. Other wet etching chemistries were possible to create a trench, such as BOE and hydrofluoric acid, due to their ability to remove SiO$_2$; however, these etchants were incompatible with other substrate materials and simply could not provide the anisotropy needed to form near vertical trench sidewalls. The solution to the issue was to place a sacrificial layer beneath the photoresist mask. Once the RIE etch was completed, the substrate could be soaked in the appropriate etchant to lift-off any contamination. This concept is shown schematically in Figure 47.

The introduction of the TiW sacrificial layer assumes that even if the photoresist “fence” structure occurs, the base of the walls will be anchored to the TiW layer and not the nanotubes or the substrate. As a result, removing the TiW layer should also
have the effect of removing any “fence” structures that appear from the RIE. It should also be noted that TiW was not chosen arbitrarily, but rather because it satisfied a set of parameters making it ideal for this application. First, TiW is often used as an adhesion layer, thus the possibility of delamination is minimal. Second, TiW can be deposited easily by electron beam evaporation or magnetron sputtering. Lastly, and perhaps most importantly, a common wet etchant for TiW is hydrogen peroxide, a chemical which is compatible with all materials on the substrate. Additionally, TiW can be etched in the RIE using CF₄ plasmas using the same plasma that performs the SiO₂ etching.

To integrate the TiW sacrificial layer into the 2nd generation fabrication process, a blanket TiW metallization is performed over the entire substrate immediately before the fourth lithographic step. Once the TiW metal is deposited to a thickness of 200 to 250 nm, positive photoresist is again patterned to form small rectangular windows over the active region of the device as shown in Figure 47. At this point there are two options on how to first remove the TiW from the open vias in order to expose the nanotubes and dielectric substrate below. The methods include a wet etch in hydrogen peroxide at 50 °C or a dry process in the RIE system using a CF₄ plasma. The wet etch method was attempted and the TiW was removed to expose the nanotubes and the substrate; however, a number of substrates showed cracking in the photoresist mask with the most severe cases exhibiting significant delamination. Since the photoresist mask was critical to the RIE process following the TiW
removal, the TiW was etched using the RIE. The etch process used to remove the TiW, excess nanotubes, and SiO₂ to define the trench structure was slightly different from previous RIE etch recipes. The process was done in two stages, without breaking vacuum. The first stage occurred at a base pressure of 50 mtorr, a CF₄ flow rate of 50 sccm, an O₂ flow rate of 10 sccm, an RIE power of 230 W, for a typical duration of 10 minutes. The etch time during this stage can vary depending upon the desired depth of the trench. The addition of the oxygen to the etch process was done to aid in the removal of the nanotubes. While the physical bombardment of the nanotubes can, in fact, remove them, the process takes an unnecessarily long time. Thus, with the addition of the oxygen, the nanotubes will also be attacked chemically, leading to a more robust etching method with a lesser possibility of nanotube remnants left behind. This first stage is the primary etching phase of the process where all of the materials that need to be removed are etched away. The second phase of the etch process is a simple cleaning step to aid in the removal of the surface particulate contamination seen in Figure 46. In this phase, the etch process occurs at a base pressure of 30 mtorr, an O₂ flow rate of 50 sccm, an RIE power of 100 W, for a duration of 5 minutes. Upon completion of the RIE process, the substrate is placed into a BOE etch for approximately 90 seconds to undercut and slightly cantilever the nanotube tips. Once the substrate is rinsed and dried from the BOE dip, it is soaked in warm acetone to remove the remaining photoresist followed by a soak in hydrogen peroxide heated to 50 °C to remove the TiW and lift off any of
the potential “fence” structures resulting from the RIE. The results of these processing steps are shown in the SEM images of Figure 48.

As can be seen in Figure 48, the RIE process successfully created a well defined trench in the active region of the device separating the anode and the cathode. Moreover, the addition of the TiW sacrificial layer eliminated the photoresist “fence” structures and significantly reduced surface contamination. Figure 48 (far right image) also shows the CNTs slightly cantilevered over the trench by the removal of SiO$_2$ during the BOE etch.

### 7.7.2 Metallic Carbon Nanotube Protective Layer

Despite the modifications to the fabrication process, a new issue was discovered. After SEM analysis of the substrates at different stages of the fabrication process, it appeared the CNTs gradually become increasingly contaminated. This can be seen in the far right image of Figure 48. If this SEM image is compared to earlier SEM images of nanotubes before they are exposed to numerous lithographic steps, a
striking difference is noted. The earlier SEM images (Figure 25, Figure 40, Figure 42, Figure 44) show relatively clean nanotubes while the nanotubes shown in Figure 48 (far right image) appear to have thicker than usual diameters and are harder to distinguish individual CNTs. On the contrary, individual nanotubes were readily observed in earlier SEM images of substrates that had not experienced any lithographic processing. To help prevent this contamination of the nanotubes another protective metal layer, typically Ti or TiW, was introduced earlier in the fabrication process to protect the nanotubes. A blanket layer of, in this case, Ti, is evaporated to a thickness of 100 nm immediately following the DEP process. In this manner, the nanotubes are encapsulated in a robust metal film thus protecting their surfaces from contamination. Other than the addition of the metal protective layer, the fabrication process remains essentially unchanged. In some instances, such as the device isolation etch and the deposition of the CNT contact layer/cathode bond pad, the Ti or TiW is first removed prior to metal deposition or etching of the Cr/Au layers. To complete the device fabrication, the metal is fully removed during the CNT cantilevering stage using dilute hydrofluoric acid (100 deionized H₂O:1 49% HF) or hydrogen peroxide. SEM images of a completed device are shown in Figure 48 and again below in Figure 49; however, this particular device did not employ the protective metal layer previously discussed. As a result, the CNT network exhibits the same surface contamination shown in Figure 48.
Figure 49: SEM images of a structurally complete device. (Left) Low magnification image of a completed device showing anode, cathode, gates, and CNT emitters. (Right) High magnification image showing the cathode and the cantilevered CNT emitter tips slightly protruding into the gap.

Figure 48 and Figure 49 the devices show structurally complete devices ready for electrical testing despite the contamination seen on the nanotubes. It should be noted that the position of the gates is likely not ideal for triode operation since they are situated behind the emitter tips. To maximize gate effectiveness they will need to be moved closer to the emitters.

### 7.8 Second Generation Electrical Testing

#### 7.8.1 Diode Configuration with Metallic Anode

The devices depicted in Figure 48 and Figure 49 were tested in a diode configuration which is shown schematically in Figure 50. The samples were placed into a vacuum chamber and brought to a base pressure of $1 \times 10^{-6}$ torr. The voltage was applied using a Keithley 237 High Voltage SMU. In diode configuration the cathode is grounded while a positive bias is applied to the anode. The gates were not used in the testing and were left floating. In order to initiate field emission, typical extraction fields are
on the order of 1-4 V/μm for vertical emitter geometries [11, 142, 143]. By comparison, the extraction fields of lateral emitters are often higher, typically on the order of 5 to 10 V/μm or more [20, 144, 145]. Given that the anode-cathode gap was on the order of 10 μm, voltages of 50 to 100 V would be expected to initiate emission.

![Electrical setups used to test the 2nd generation of DEP devices. The tests were conducted in a diode configuration with a positive potential applied to the anode, the cathode held at ground, and the gates left floating. The testing was completed in a vacuum chamber at a base pressure of 1×10⁻⁶ torr.](image)

However, even when the anode voltage rose above 250 V, creating fields in excess of 25 V/μm, no field emission was observed. Though it is difficult to determine why the devices would not emit at such large electric fields, numerous theories were considered. One possibility is that emission does occur; however only briefly, and results in the immediate charging of the surrounding dielectric medium. As charge builds up in the vicinity of the emitters, the potential at the CNT tips is reduced. As this process continues the potential at the tips eventually drops below an emission threshold and emission ceases. This very brief emission is not detected by the instrument because the charging of all the stray capacitances of the metal conductors...
leading up to the device dwarfs the capacitance generated by the anode and cathode, and thus it is not detected.

The anode itself may also pose a problem due to the significant sputtering of Au during the RIE process. The removal of the Au reduces the cross sectional area of the anode’s leading edge closest to the cathode, and hence produces a smaller collector for the electrons. All of these factors, in addition to the large anode-cathode separation (10 μm) and the potential nanotube contamination, severely limited the capability of the device to field emit electrons.

7.8.2 Diode Configuration with Silicon Anode

To improve the likelihood of emission, the final RIE process was modified slightly. In this new configuration, the RIE etch process would essentially remain the same except the SiO₂ layer would be etched to within 50 to 100 nm of the underlying silicon substrate. Following the RIE, a 90 second BOE etch would not only cantilever the CNT emitters, but also remove the remaining SiO₂ and expose the Si surface below.
The exposed Si surface is then used as the anode. Utilizing the silicon as the anode addresses many of the issues hindering emission. The anode is larger and much closer than the original design which will result in lower applied voltages and a larger anode area for electron capture. Additionally, by removing a large area of SiO$_2$ from the vicinity of the emitters, charging is greatly reduced. This new device design is shown schematically in Figure 51.

Using samples from the same fabrication run, the new RIE process and BOE etch were implemented. Contact to the Si, and hence the anode, is made through the backside of the wafer using conductive silver paint. The Si used for the fabrication was low resistivity thus good electrical contact is achieved simply by using conductive paint. Once the fabrication is complete, the sample is placed into a vacuum chamber and brought to a base pressure of 1×10$^{-6}$ torr. Electrical contact is then made to the Si anode and cathode while leaving the gates and the original metallic anode floating (Figure 52).
Similar to earlier electrical tests, a positive potential is applied to the anode while the cathode is grounded. In this configuration field emission was achieved.

**7.8.3 Current-Voltage and Fowler-Nordheim Analysis**

To examine the current-voltage (I-V) characteristics a series of voltage sweeps were performed using a Keithley 237 SMU. Throughout these sweeps, the voltage was swept from zero to typically 150 V while simultaneously measuring the current through the anode.
Figure 53: Current-voltage characteristics of a typical DEP based device operating as a diode utilizing a silicon anode as shown in Figure 52. (Inset) Corresponding Fowler-Nordheim plot generated from the I-V data.

Figure 54: Current-voltage characteristics of a typical DEP based device operating as a diode utilizing a silicon anode as shown in Figure 52. (Inset) Corresponding Fowler-Nordheim plot generated from the I-V data.
Typical field emission results are shown in Figure 53 and Figure 54 for two different devices, S13-L3 and S13-L4, operating in a diode configuration (Figure 52). In both instances, the I-V plot shows an exponential rise in anode current as a function of electric field. Moreover, from the Fowler-Nordheim plots (insets) the onset of field emission can identified by the data points at the bottom of the negatively sloped linear fit. The turn-on field for these particular devices was approximately 25 V/μm, significantly higher than vertical emitters (1 to 4 V/μm) and even lateral emitter geometries (5 to 10+ V/μm). The turn-on field is defined here as the macroscopic electric field required to draw 1 nA of current through the anode. In addition to requiring large electric fields, the devices were also unable to handle large currents and often failed when emitting above ~50 nA. Comparing these values to current research with lateral CNT emitters reveals a significant gap in device performance in both threshold fields, which are typically 4-10 V/μm [20, 145]. To produce a viable device these parameters will undoubtedly need improvement.

Figure 55 shows an SEM image of each device just prior to the field emission experiments. In both cases, the CNTs can be seen to approach, and in some instances, protrude from the edge of the trench. The contamination present on the nanotube surfaces, likely from exposure to photoresist chemistries and RIE processing, is noted. The silicon anode shows interesting surface morphology. While the composition of the surface was not examined, the pitted features suggest micro-
masking, likely from residues generated by the CF$_4$ plasma used to etch the SiO$_2$ from the trench region. The point is supported further in the SEM of S13-L3 in Figure 55 where small deposits of material can be seen due to the high tilt angle. Despite the presence of this contamination, field emission was successful, though device performance can be improved.

In addition to the I-V plots of Figure 53 and Figure 54, a Fowler-Nordheim (F-N) plot was calculated for each, shown in the inset of both figures.

The F-N plots are shown again in Figure 56 with the addition of the linear fit data which will be used to estimate the electric field enhancement factor, $\gamma$. To construct the F-N plots, $\ln \left[ J/F_0^2 \right]$ is plotted against $1/F_0$ with the result being a straight line if well behaved field emission is generated.
To calculate these plots in accordance with Equation 7 and Equation 8 a few geometrical assumptions are needed. First, the cross-sectional area of the nanotube emitter must be calculated. It is estimated that the CNT mat thickness is approximately 50 nm while its width is 6 μm. This results in an estimated emitting area of $\sim3\times10^{-13}$ m$^2$. The other assumption is based on the anode-cathode separation distance, which will be needed to calculate $F_0$. Although the trench is approximately 1.2 μm deep, the presence of the Si surface contamination makes it difficult to assess exactly where the anode begins. As a result, the anode-cathode “gap” is taken to be 5 μm in this set of calculations. Lastly, the electronic work function of the carbon nanotubes is taken as 4.5 eV [146, 147].
In both the plots in Figure 56, a well defined line with a negative slope is formed by the data of interest. This result suggests that the current measured was the result of field emission and not another phenomenon. The extraneous data to the right of the blue line (indicating the linear fit) is not included in the linear fit data set since it does not correspond to any actual field emission. Only data points where emission occurs are factored in to the linear fit. From the fit data, the electric field enhancement for each device may be estimated according to Equation 11. For S13-L3 the following is obtained for the electric field enhancement factor.

\[
\gamma = \frac{C \phi^{3/2}}{m} \rightarrow \gamma = \frac{(6.8309 \times 10^9)(4.5^{3/2})}{-4.496 \times 10^8} \rightarrow \gamma = 145
\]

Equation 19

And for S13-L4 the following is obtained in the same manner.

\[
\gamma = \frac{C \phi^{3/2}}{m} \rightarrow \gamma = \frac{(6.8309 \times 10^9)(4.5^{3/2})}{-5.492 \times 10^8} \rightarrow \gamma = 118
\]

Equation 20

Comparing these experimentally obtained values to those found in the literature reveals a relatively weak field enhancement at the CNT tips. Typical values of \( \gamma \),
assuming robust field emission from clean CNTs, typically range from 500 up to a few thousand [148]. As a result of the weak enhancement, higher fields are needed to initiate field emission, as evidenced by the 25 V/μm turn-on fields exhibited by these devices.

The large electric fields needed for field emission, coupled with the proximity of the metallic cathode to the trench edge, raised concerns about where the emission was localized. It was plausible, unless proven otherwise, that the emission originated from the edge of the metal and not the tips of the CNTs. To disprove this hypothesis a sample geometrically identical to S13-L3 and S13-L4 but without nanotubes was tested. On this particular sample, the metallic conductor was approximately 1 μm from the edge of the trench, similar to the samples shown in Figure 55. The electrical test setup was also the same as Figure 52 and the testing was performed in a vacuum chamber at a base pressure of 1×10⁻⁶ torr. The experiment did not demonstrate any field emission to the Si anode, despite voltages more than twice that required by S13-L3 and S13-L4 for emission (~250-300V). This experiment was repeated numerous times on other samples with the same result. The conclusions from this set of tests confirmed that the emission current from S13-L3 and S13-L4 originated from the nanotubes in the form of field emission.
7.9 Angled Evaporation and Future Implications

Given the success of the S13-L3 and S13-L4 samples, further refinements to the fabrication process were made in an attempt to improve device performance. Overall, the process remained the same; however, based on the success of using the silicon anode, a method for placing the metallic anode closer to the cathode was needed. The primary reason for this was the impractical nature of using the bulk silicon substrate as the anode since it would be difficult to isolate each anode. A possible solution would be to use silicon-on-insulator substrates; however, these substrates are often more expensive than standard silicon or quartz wafers and add additional complexity to the fabrication process.

From the results of electrical tests discussed in Section 7.8.1 it was clear that the original metallic anode was not suitable due to its distance from the cathode and the severe damage it experiences during the RIE. To resolve this issue, a new anode needed to be created much closer to the cathode. Originally thought to be a difficult proposition, the solution proved to be relatively simplistic and easily integrated into the current fabrication process. The solution would utilize the highly directional deposition of electron beam evaporation, a substrate mounted at an angle other than 90 degrees with respect to the incident evaporated material, and a shadowing structure present in the device geometry.
Preliminary tests have been completed on the possibility of performing an angled evaporation. Though the crucible in the evaporator containing the metal to be deposited remains fixed, the sample receiving the metal deposition is mounted at an angle within the chamber, denoted by $\alpha$ in Figure 57A. Given the extremely high directionality of the evaporation process, the tilted substrate can be oriented in such a way that surface topography will result in a shadowing effect as shown in Figure 57B. In this SEM image, the height of the shadowing structure was approximately 700 nm and the angle of evaporation was 45 degrees. This led to a lateral separation between the two metallic films of about 700nm, as calculated geometrically. Since the anode-cathode gap can be controlled strictly on the angle of evaporation, $\alpha$, and the height of the shadowing structure, $h$, small gaps can be fabricated without the need for time consuming serial processes such as electron beam lithography. Initial tests have shown this process to work very well at fabricating gaps approximately 2 $\mu$m or less at angles of 45 and 60 degrees.

![Figure 57: (A) Schematic illustration showing a cross-sectional view of the angled evaporation process. Note that the separation between the metal films can be entirely controlled by the angle of evaporation, $\alpha$, and the height of the shadowing structure, $h$. (B) SEM image showing the results of proof-of-concept test for the angled evaporation process. The shadowing structure is approximately 700 nm in height and the angle of evaporation was 45 degrees.]
Given the successful results of these preliminary tests, the concept was integrated into the fabrication process for the DEP-based device. The final step of the fabrication process (RIE etch of SiO₂), shown in Figure 58A, allows the possibility of also using the photoresist / TiW mask as a shadowing structure to create an anode significantly closer to the CNT emitters. The photoresist and the TiW would then be used as a lift-off layer to define the new anode structure. Figure 58B shows the final device concept once the angled evaporation has been completed.

![Figure 58: (A) Diagram of device showing the photoresist shadowing structure used in the angled evaporation process. (B) Device following the lift-off of the photoresist mask and the TiW protective layer leaving behind an anode that is significantly closer to the CNT emitters.](image)

Though this process was attempted numerous times, none produced a device that had both a well defined anode and CNT emitter structures capable of field emission. In most instances; however, the angled evaporation was successful, but the subsequent processing caused contamination of the emitters resulting in devices unable to field emit. Yet, the importance of the proficiency gained by performing multiple angled evaporations cannot be diminished. The results and experience gained during these
experiments would eventually allow the angled evaporation to be the critical processing step in fabricating a new type of CNT-based field emission device.

### 7.10 Conclusions for DEP Devices

Before discussing the next evolution of CNT field emission devices, a summary of the DEP based devices addressing some of the technical hurdles and potential solutions is needed. Overall, the devices that were successfully operated as diodes exhibited device performance lower than similar work found in literature. The reduced device performance can be attributed to many factors.

#### 7.10.1 Carbon Nanotube Contamination

As discussed in previous chapters, carbon nanotubes are susceptible to contamination from exposure to photoresist and the related chemistries. Although steps to reduce this contamination were implemented into the fabrication process, there was still not a reliable method to keep the CNT tips sufficiently clean. Typically, the CNT network was buried in a metallic layer to protect the surfaces; however, this layer could not fully protect the emitter tips during the RIE etch process. As a result, the tips likely became contaminated by the fluorinated byproducts of the etch, thus contributing to degraded device performance.

#### 7.10.2 Carbon Nanotube Cantilevering

Initial electrical tests showed that the tips of the carbon nanotubes must be cantilevered in order to field emit. Ideally, the final structure adopts a “diving board”
structure. However, cantilevering the nanotubes in such a manner proved very difficult primarily due to the small, yet critical, variance from device to device. Thus a particular BOE etch duration may be ideal for certain devices but either too long or too short for others. These difficulties are shown in the SEM images of Figure 59A-C.

### 7.10.3 Emitter Edge Definition

Adding to the cantilevering difficulties was the inability to produce a well defined emitter edge. Although the oxygen plasma etching of the nanotubes was successful, it was unable to produce perfectly straight edges.

![Figure 59: SEM images illustrating the cantilevering non-uniformities at the CNT emitter tips. Though the variance is small in one instance (A), the other samples (B,C) exhibit jagged edges.](image)

It is plausible that the plasma randomly attacks regions of the nanotube network resulting in structures shown in Figure 59A-C. Other possibilities include degradation of the protective etch masks during RIE or the actual fracture of the nanotube network due to excessive cantilevering.
7.10.4 Electrical Performance Limits

The devices that were successfully operated as diodes also elucidated what may be practical limits to the electrical performance of this class of device in its current form. Taking an estimate of the cross-sectional area of the nanotube network (50 nm thick \( \times \) 6 \( \mu \)m wide) to be \( 3 \times 10^{-13} \) m\(^2\), or \( 3 \times 10^{-9} \) cm\(^2\), it becomes apparent that the device will not be able to carry large currents. Given the small emission cross-section, the current densities will be high; however, the total current through a single device will be relatively limited. Practically, this can be overcome by placing many devices in parallel; however a better solution would be to produce a device that is capable of higher total currents without jeopardizing device lifetime. This will preclude this device from operating in systems requiring high power and may limit it to low power applications only.

The effectiveness of the gates, though remaining untested, is also a concern. Given the current fabrication process and current fabrication limitations, the gates can be placed to within a few microns of the nanotube tips. This relatively large distance may severely reduce the ability of the gates to modulate the local electric field at the emitters causing reduced device performance. The gates can be patterned significantly closer using other methods such as electron beam lithography; however, this would introduce a time consuming, serial processing step, which is contrary to the goals of this research.
8 Thermal Chemical Vapor Deposition Based Devices

Despite the lower than expected performance of the DEP-based devices, the discoveries made while fabricating and testing proved invaluable in the creation of an entirely new device concept. This new concept is based on the chemical synthesis of the CNT emitter structure via thermal chemical vapor deposition (TCVD) methods. Thermal CVD relies on the in-situ growth of the nanotubes to form the emitter structure rather than the physical deposition and subsequent processing techniques used to define the emitter in the DEP based devices.

8.1 Device Concept

While the initial TCVD device concept is remarkably similar to the DEP version, the fabrication processes are significantly different. Perhaps the most important difference is the process step when the carbon nanotubes are deposited/grown in the fabrication process. For the DEP version, the CNT deposition was one of the first steps since additional processing on the nanotubes was necessary to define the emitter structure. As a result, the CNTs often became contaminated if not sufficiently protected. To the contrary, the TCVD version performs the nanotube synthesis, or growth, during the final processing step, thus the nanotubes are free of process induced contaminants. Furthermore, the TCVD process is also inherently clean due to the high temperatures reached during the CNT growth.
The basic device concept for the TCVD device is shown in Figure 60, again in a triode configuration with an anode, cathode, and gate. Though geometrically similar to the DEP devices, the main difference is the cathode. Here, the cathode consists of three layers of metal with the middle layer being a transition metal catalyst suitable for CNT growth. The metal layer below the catalyst functions as a diffusion barrier while the topmost layer caps the catalyst and prevents unwanted nanotube growth perpendicular to the chip surface.

Figure 60: Schematic showing the basic concept for the lateral TCVD version of the triode.

However, before a full fabrication process was developed for the device concept in Figure 60, a series of preliminary proof-of-concept experiments were performed.

### 8.2 Lateral Nanotube Growth from Catalyst Metal Stacks

#### 8.2.1 Ti / Ni / Ti Metal Trilayer

From Figure 60 it is evident that the success of this particular device will critically depend on the ability to successfully grow carbon nanotubes laterally from the side
of the exposed catalyst. Although the metal catalysts capable of nanotube growth are known, the correct combination of materials and thicknesses needed to be determined experimentally.

The first metal combination was a combination of titanium and nickel. Using a silicon substrate, 200 nm of Ti was evaporated followed by 100 nm of Ni, followed by 200 nm of Ti. The silicon wafer was then removed from the evaporator and cleaved to expose a Ti / Ni / Ti edge. The growth process used can be summarized in Table 4.

Table 4: Summary of thermal CVD growth process used for the Ti / Ni / Ti trilayer experiment.

<table>
<thead>
<tr>
<th>Time Elapsed (hrs):(min):(sec)</th>
<th>Description</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>0:00:00</td>
<td>Begin heating to growth temperature in air</td>
<td>730°C</td>
</tr>
<tr>
<td>0:30:00</td>
<td>Ar gas flow begins</td>
<td>1200 sccm</td>
</tr>
<tr>
<td>0:45:00</td>
<td>H₂ gas flow begins</td>
<td>500 sccm</td>
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<tr>
<td>0:45:00</td>
<td>Ar gas flow reduced</td>
<td>800 sccm</td>
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<tr>
<td>0:55:00</td>
<td>H₂ gas flow ends</td>
<td>0 sccm</td>
</tr>
<tr>
<td>0:55:00</td>
<td>Ar gas flow increased</td>
<td>1200 sccm</td>
</tr>
<tr>
<td>0:55:00</td>
<td>C₂H₂ gas flow begins</td>
<td>15 sccm</td>
</tr>
<tr>
<td>0:57:00</td>
<td>C₂H₂ gas flow ends</td>
<td>0 sccm</td>
</tr>
<tr>
<td>0:57:00</td>
<td>Furnace cools down</td>
<td>23°C</td>
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</table>

Once removed, the samples are examined by SEM. The results are shown in Figure 61.
In the SEM images it is clear that the nanotubes grew in a well-controlled manner to form an array along the exposed Ni edge. Despite the successful results, further tests were performed to ascertain if a metal combination existed that was capable of even more robust CNT growth.

### 8.2.2 Cr / Fe / Cr Metal Trilayer

The next metal combination was a combination of chromium and iron. In this instance two types of samples were created with different thicknesses of the iron layer. Again using a silicon substrate, a generic lithographic pattern was generated prior to evaporation of the metals. This allows the examination of both a cleaved edge and also a lithographically defined edge. The samples are then placed into an evaporator and 30 nm of Cr is evaporated, followed by either 100 nm or 2.5 nm of Fe, followed by 100 nm of Cr. The silicon wafer was then removed from the evaporator and cleaved to expose a Cr/Fe/Cr sidewall. Small samples were then loaded into a quartz tube furnace and the carbon nanotube growth process was
initiated. The growth process is summarized in Table 5. The results from the two different types of samples are shown in Figure 62.

Table 5: Summary of thermal CVD growth process used for the Cr/Fe/Cr trilayer experiment.

<table>
<thead>
<tr>
<th>Time Elapsed (hrs):(min):(sec)</th>
<th>Description</th>
<th>Parameter</th>
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<tbody>
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</tr>
<tr>
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</tr>
<tr>
<td>0:45:00</td>
<td>H₂ gas flow begins</td>
<td>500 sccm</td>
</tr>
<tr>
<td>0:45:00</td>
<td>Ar gas flow reduced</td>
<td>800 sccm</td>
</tr>
<tr>
<td>0:55:00</td>
<td>H₂ gas flow ends</td>
<td>0 sccm</td>
</tr>
<tr>
<td>0:55:00</td>
<td>Ar gas flow increased</td>
<td>1200 sccm</td>
</tr>
<tr>
<td>0:55:00</td>
<td>C₂H₂ gas flow begins</td>
<td>15 sccm</td>
</tr>
<tr>
<td>2:55:00</td>
<td>C₂H₂ gas flow ends</td>
<td>0 sccm</td>
</tr>
<tr>
<td>2:55:00</td>
<td>Furnace cools down</td>
<td>23°C</td>
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</table>

From the SEM images it is apparent that the combination of Cr/Fe/Cr does not produce acceptable CNT arrays. For the set of samples with 100 nm of Fe (Figure 62, top), there are regions where minimal nanotube growth was seen; however, these regions of nanotube growth were often spread randomly along the edge making it unreliable for use in device fabrication. The set of samples with only 2.5 nm of Fe catalyst (Figure 62, bottom) showed very sparse CNTs on the edge. The only nanotubes that are seen were located on a region of the Cr where the metal had peeled from the substrate. In both cases, there appeared to be little difference between the growths done on cleaved edges versus those done on lithographically defined edges.
Figure 62: SEM image showing carbon nanotubes grown laterally from a Cr/Fe/Cr metal stack deposited on a silicon substrate. Shown are examples of growth from both a cleaved metal edge and a lithographically defined metal edge.

8.2.3 SiO₂ / Fe / SiO₂ Trilayer

The final combination did not use three metallic layers, but rather sought to sandwich the catalyst between thermally grown and sputtered SiO₂ layers. To create such a structure, a silicon wafer is first thermally oxidized to a thickness of 600 nm. Following the oxidation, the substrate is placed into an evaporator and 100 nm of Fe is deposited. After the iron deposition, the sample is loaded into a sputtering system and an additional 250 nm of SiO₂ is deposited. One the deposition process is
complete, the samples are placed into a quartz tube furnace and the CNT growth initiated. The growth process used is identical to the one done with previous sets of samples with the only difference being the duration during which the acetylene is flowing. In this case, the acetylene is allowed to flow for either 1 hour or 2 hours. The results of the 1 hour growth are shown in Figure 63.

![Figure 63: SEM images showing carbon nanotubes grown laterally for 1 hour from a SiO$_2$/Fe/SiO$_2$ stack. Shown is a growth from a cleaved edge. It should be noted that the 250 nm sputtered SiO$_2$ was not sufficient in preventing the nanotubes from growing up through it. This is likely due to pinholes in the SiO$_2$ and morphology changes due to the high growth temperature.](image)

The 1 hour growth was relatively successful at producing nanotubes; however, the nanotubes were not confined to the metal edge. Instead, the nanotubes grew through the 250 nm SiO$_2$ layer put in place to prevent such an occurrence. Possible explanations include pinholes in the sputtered SiO$_2$ and micro-cracking/morphological changes resulting from the high growth temperature. In both instances, the acetylene gas would have access to the metal catalyst, giving rise to nanotube growth. Moreover, there also appears to be some amorphous carbon material deposited along the exposed Fe edge (Figure 63, far right). Typically, nanotubes are grown from very thin catalyst layers, often less than 10 nm. With such
a thin film, the high temperatures cause the catalyst to form small nanoparticles which act as nucleation sites from which nanotubes grow. In the samples shown in Figure 63 (and Figure 64) the Fe catalyst layer is 100 nm thick, and while not a true bulk surface, it will likely not exhibit the same ideal nanostructure needed to facilitate robust nanotube growth.

While the 1 hour growth showed some success, the 2 hour growth exhibited significantly greater amounts of amorphous carbon deposits. Again, nanotubes perforated the 250 nm SiO₂ capping layer; however the most significant growth was seen along the cleaved edge.

In Figure 64, large protrusions appear to be emanating from the edge of the sample. Although a materials characterization was not performed, as this was not the purpose of the experiment, it is theorized that the protrusions consist of some nanotubes but
primarily amorphous carbon deposits. This observation is in line with results from the shorter 1 hour growth where the initial signs of these deposits were seen to a lesser degree.

### 8.3 First Generation Devices

#### 8.3.1 Fabrication Process

With the results of the lateral growth of carbon nanotubes from catalyst metals stacks indicating Ti/Ni/Ti as the best combination, fabrication to create a device similar to the one shown in Figure 60 proceeded. The fabrication process is summarized in Table 6 and followed by schematics illustrating the results of the fabrication at various steps.

**Table 6: Summary of the fabrication process for the first generation CVD based devices.**

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Clean thermally oxidized Si wafer; load into evaporator</td>
<td>NA</td>
</tr>
<tr>
<td>2</td>
<td>Evaporate 100nm Ti over entire surface</td>
<td>NA</td>
</tr>
<tr>
<td>3</td>
<td>Pattern photoresist and etch Ti using dilute HF</td>
<td>NA</td>
</tr>
<tr>
<td>4</td>
<td>RIE etch of SiO$_2$ layer: 50 mtorr, CF$_4$ flow of 50 sccm, 230 W, 5-10 minutes</td>
<td>Figure 65</td>
</tr>
<tr>
<td>5</td>
<td>BOE etch to remove remaining SiO$_2$</td>
<td>Figure 65</td>
</tr>
<tr>
<td>6</td>
<td>Removal of Ti and photoresist; cleaned in piranha solution (H$_2$O$_2$ and H$_2$SO$_4$)</td>
<td>NA</td>
</tr>
<tr>
<td>7</td>
<td>Pattern photoresist to form cathode</td>
<td>NA</td>
</tr>
<tr>
<td>8</td>
<td>Evaporate cathode and gate metal: 200nm Ti, 100nm Ni, 200 nm Ti; lift off process</td>
<td>Figure 66</td>
</tr>
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Figure 65: Cross-section and top-down views of the substrate after the first lithographic step. Here, a small rectangular window is opened in the photoresist and Ti layers to expose the SiO₂ below. The photoresist and Ti layers will serve as an etch mask for an RIE process which will remove the majority of the SiO₂. A brief BOE etch will be performed to complete the removal of the SiO₂.

Figure 66: Cross-section and top-down views of the substrate after depositing the Ti/Ni/Ti layer that forms the cathode.

With all of the device electrodes in place, the substrate is ready for the nanotube growth process. The nanotubes were grown using thermal chemical vapor deposition and requires an experimental setup similar to that shown in Figure 9. The final device structures are shown schematically in Figure 67. The CNT growth process is outlined in Table 7.
Figure 67: Schematic illustrating the anticipated final device for the first generation of thermal CVD based devices.

Table 7: Summary of thermal CVD growth of CNTs for the first generation of devices.

<table>
<thead>
<tr>
<th>Time Elapsed (hrs):(min):(sec)</th>
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<td>Furnace cools down</td>
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After the nanotube growth process, it was apparent that the final Ti layer was not sufficient in hindering unwanted stray nanotube growth. Much like the Fe catalyst was able to grow nanotubes through the sputtered SiO₂, the Ni catalyst was also able to grow nanotubes through the 200 nm Ti layer. Thicker Ti layers were also used, but were unable to successfully hinder the unwanted CNT growth from below. SEM images showing the results of the nanotube growth are shown in Figure 68. Each nanotube region is approximately 8 μm wide and 5 μm tall. This phenomenon was consistent for each nanotube growth (using the fabrication process for this device design) as numerous batches of samples were fabricated using the same growth process.
Figure 68: SEM images of the first generation thermal CVD devices after the nanotube growth process. The nanotubes are seen having grown through the 200 nm Ti layer put in place to prevent such growth from occurring.

8.3.2 Electrical Testing

To test the devices, they were placed into a vacuum chamber and brought to a base pressure of $1 \times 10^{-6}$ torr. A high voltage SMU was then connected as shown in Figure 69.

Figure 69: Electrical setup used to test the completed first generation devices in a simple diode configuration.
A positive potential is applied to the silicon anode while the cathode remains grounded. The applied voltage was then increased slowly while simultaneously measuring the anode current. Though many I-V sweeps were performed on numerous samples, typical I-V data, along with the corresponding Fowler-Nordheim plot, is shown in Figure 70. The plot of the I-V characteristics exhibits a very rapid, exponential rise in emission current as a function of electric field, indicative of field emission. However, the electric fields needed to initiate emission are also relatively high in comparison to values found in literature. Given the morphology of the cathode, the relatively high electric fields are not surprising. It was originally theorized that the nanotubes would only grow laterally from the edge of the exposed Ni catalyst. While this may have occurred, the nanotubes also grew from all other cathode surfaces. The result, as shown in Figure 68, is a tangled nanotube array with randomly oriented tips. It is likely that such an array, due to the high density of nanotubes and the orientations of their tips, will result in a high degree of nanotube-nanotube screening. Due to the increased screening, higher electric fields are necessary.
Figure 70: Current-voltage characteristics of a device operating in a diode configuration. (Inset) Corresponding Fowler-Nordheim plot generated from the I-V data.

By making some estimates (based on SEM images) of the typical device geometry, a F-N plot (inset Figure 70) can be generated. The necessary parameters are the emitting area, and the anode-cathode separation. Using estimates for the nanotube height and emitter width, 5 μm and 8 μm respectively, an approximate emitting area of $4 \times 10^{-11}$ m$^2$ is obtained. The anode-cathode gap is again difficult to estimate since it is unknown which nanotubes are participating in the emission or what distance from the SiO$_2$ sidewall the anode becomes. As a rough estimate, the anode-cathode gap is taken to be 5 μm. With this data, a F-N plot was generated to validate the field emission and estimate the electric field enhancement factor. Taking a linear fit of the relevant emission data (again, only data points corresponding to an actual current are
included in the linear fit) yields a straight line that is in good agreement with the experimental data.

Based on the slope of the linear fit, an estimate of the field enhancement factor can be obtained. Again, given the earlier estimates regarding device geometry, this result is only an approximation. Using Equation 11 the electric field enhancement factor can be estimated as

$$\gamma = \frac{C \phi^{3/2}}{|m|} \rightarrow \gamma = \frac{(6.8309 \times 10^9)(4.5^{3/2})}{-1.6614 \times 10^8} \rightarrow \gamma = 392$$

Equation 21

Though not indicative of exceptional field enhancement, a value of 392 is a more than twofold improvement when compared to DEP-based devices (enhancement factors of 145 and 118). Further improvements to the nanotube morphology to reduce screening effects and modifications to the growth process to produce straighter nanotubes should result in larger field enhancement factors and high performance devices.
8.4 Second Generation Devices

8.4.1 Device Modifications

To this point, all attempts at utilizing thermal CVD as a nanotube growth mechanism sought to grow the nanotubes laterally from the exposed edge of a metal trilayer. While in principle, this is possible, in practice it proves difficult to achieve consistent results. Typically, some devices would exhibit nanotubes likely to field emit, while other samples would not show sufficient nanotube growth at all. The reasons behind this are twofold. Since the metal trilayer is fabricated using a lift-off process, the edge of the metal catalyst (Ni) responsible for growing the nanotubes is in contact with the photoresist. Typically, the photoresist is simply dissolved away using acetone during the lift-off, but since the cleanliness of the catalyst surface is paramount to a successful nanotube growth, any residue, no matter how minute, can greatly affect the results. As a result, a method of depositing the catalyst without having it contact any possible sources of contamination is necessary. The second issue hindering the nanotube growth is the catalyst layer itself. For most applications involving nanotube growth, a thin catalyst layer, typically ~5 nm, is deposited onto a substrate and then the nanotubes are grown from this layer. During the growth process, the thin catalyst layer breaks up into small islands that essentially determine the diameter of the nanotubes being grown [149]. This is possible only because the catalyst film is exceedingly thin. In the metal trilayer used in the first generation devices, the catalyst film does not have the ability to form small islands. Though it is
thin in the vertical direction (~100 nm), it is “thick” in the plane of the substrate, making it appear more like a bulk surface. As a result, the nanotube growth from such surfaces is heavily dependant on the nanoscale surface morphology of the edge of the catalyst layer. While some have found methods for treating the catalyst edge to improve nanotube growth [20], this too is tricky, and can have significant variance from device to device. Given the success and reliability shown by nanotube growth from thin catalyst layers, a method for creating a device using such catalyst layers is also desirable.

From these observations, an entirely new device concept was developed that would employ techniques learned from the DEP-based devices coupled with the more robust and reliable thermal CVD nanotube growth. A schematic of the new device is shown in Figure 71.
Utilizing the angled evaporation technique explored while fabricating the DEP-based devices, this new device concept seeks to metalize both sidewalls of an etched trench with only one sidewall containing a catalyst capable of nanotube growth.

The advantages offered by such a device are numerous. By metalizing the sidewall, the difficulties of growing nanotubes laterally from a metal trilayer are eliminated. Instead, the nanotubes will be grown perpendicular from a catalyst surface, a method that is far more robust than edge growth methods. The metallization of the sidewall also necessitates a completely dielectric substrate since the trench will have to be on the order of 10 μm deep (or greater), far greater than any thermal SiO₂ layer. Other deposited or spin-on dielectrics are feasible, but the potential for pinholing, cracking due to film stress, electrical shorts created by metal spiking at the high growth temperatures, and poor dielectric performance make them undesirable. Thus, using an entirely dielectric substrate, such as quartz, is a solution. Furthermore, the high temperature stability of quartz makes it ideal given the ultimate goal of fabricating a field emission device capable of high temperature operation.

The new design also offers advantages in fabrication. Though not excessively complex, the fabrication of the DEP-based devices involved numerous steps. In contrast, the fabrication process for a thermal CVD based device is relatively simple since it consists of a maximum of three lithographic steps, assuming a triode
geometry. Before such a device can be created, the ability to metalize a sidewall successfully must be demonstrated.

### 8.4.2 Sidewall Metallization

To test the ability to successfully combine photolithography and angled evaporation, a trench was first etched to a depth of approximately 15 μm into a quartz substrate using a photoresist/Ni mask and an RIE etch process employing CF₄ plasma. Details of these processes will be given in the fabrication process of the actual device as they do not differ. Once the trench is etched, the masking layer is removed and a layer of negative photoresist is patterned as shown in Figure 72. The sample is then mounted at 45°, placed in an evaporator, and 1 μm of Ti is deposited. The unwanted metal is then removed via lift-off.

![Figure 72: Schematic showing a top-down view of the photoresist pattern (Left) before the angled evaporation/sidewall metallization and (Right) after.](image)

The resulting structure is shown schematically in Figure 72 (right) and in SEM images of Figure 73. It is clear from the SEM images that the sidewall can be metalized successfully while maintaining continuity of the metal film as it curls over the lip and down into the trench. The continuity of the film is of critical importance as the device will not function unless a potential can be applied to the electrodes.
With the sidewall metallization technique validated, the design and fabrication of an actual device proceeded.

### 8.4.3 Fabrication Process

To fabricate the new device in a diode configuration only two lithographic steps, using standard photolithography and MEMS processing techniques, are required. By an additional lithographic step (Step 7), gates can be patterned resulting in a triode architecture. The fabrication process used to create the second generation CVD based devices is given in Table 8 and illustrated schematically in Figure 74.

**Table 8: Summary of fabrication process for the 2nd generation CVD devices.**

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Evaporate 30 nm Cr and 200 nm Au onto quartz substrate</td>
<td>Figure 74A</td>
</tr>
<tr>
<td>2</td>
<td>Lithographically pattern photoresist; electroplate Ni to a 2-3 μm thickness</td>
<td>Figure 74A</td>
</tr>
<tr>
<td>3</td>
<td>Remove photoresist with acetone; wet etch exposed Cr and Au</td>
<td>Figure 74A</td>
</tr>
<tr>
<td>4</td>
<td>RIE etch to form a trench with 1:1 aspect ratio: 50 mtorr, CF4 flow of 50 sccm, O2 flow of 3 sccm, 230 W RIE power, 100 W ICP power, 8 hours</td>
<td>Figure 74B</td>
</tr>
<tr>
<td>5</td>
<td>HF wet etch with sonication to smooth pit bottom: 45-60 seconds</td>
<td>Figure 74B</td>
</tr>
<tr>
<td>6</td>
<td>Pattern 4 μm thick, negative photoresist</td>
<td>Figure 74C</td>
</tr>
<tr>
<td>7</td>
<td>Angled evaporation at 45°: 300-700 nm Ti, lift-off process</td>
<td>Not shown</td>
</tr>
<tr>
<td>8</td>
<td>Pattern 4 μm thick, negative photoresist</td>
<td>Figure 74C</td>
</tr>
<tr>
<td>9</td>
<td>Angled evaporation at 45°: 100 nm Ti, 5 nm Ni</td>
<td>Figure 74D</td>
</tr>
<tr>
<td>10</td>
<td>Sample rotated 180°, angled evaporation at 45°: 700 nm Ti, lift-off process</td>
<td>Figure 74E</td>
</tr>
</tbody>
</table>
After lift-off, the quartz substrate is diced into smaller die and the die are loaded into a 2” diameter quartz tube furnace for the CNT growth process (Figure 74F). The details of the process are summarized in Table 9.
Table 9: Thermal CVD growth process used to fabricate 2\textsuperscript{nd} generation devices.

<table>
<thead>
<tr>
<th>Time Elapsed (hrs):(min):(sec)</th>
<th>Description Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>0:00:00</td>
<td>Evacuate furnace tube to ~10 torr, backfill with Ar</td>
</tr>
<tr>
<td>0:00:00</td>
<td>Repeat purging process</td>
</tr>
<tr>
<td>0:00:00</td>
<td>Begin heating to growth temperature</td>
</tr>
<tr>
<td>0:00:00</td>
<td>Ar gas flow begins</td>
</tr>
<tr>
<td>0:00:00</td>
<td>H(_2) gas flow begins</td>
</tr>
<tr>
<td>0:30:00</td>
<td>C(_2)H(_2) gas flow begins</td>
</tr>
<tr>
<td>0:30:30</td>
<td>C(_2)H(_2) gas flow ends</td>
</tr>
<tr>
<td>0:30:30</td>
<td>Furnace cools down</td>
</tr>
</tbody>
</table>

The initial pump and flush technique is important to ensure the CNTs only grow from the exposed Ni. Previous tests showed that samples heated in air resulted in CNTs growing up through the Ti capping layer, likely due to morphology changes in the Ti layer from the oxidation, then reduction, during the growth process. Following the purging process the growth process proceeds normally. As a result, CNTs grow from the exposed Ni along the trench sidewall but are prevented from growing elsewhere by the Ti capping layer. The results of the fabrication and growth processes are shown in the SEM images of Figure 75.
Figure 75: SEM images showing a completed second generation thermal CVD based device in a diode configuration. In both images, the nanotubes can be seen having grown from the sidewall of the cathode only without having grown from the anode or up through the Ti capping layer.

8.4.4 Electrical Testing

Field emission performance of the device in a diode configuration was characterized at room temperature and under a pressure of $1 \times 10^{-6}$ torr. The emission current was measured by a Keithley 237 High Voltage SMU as a function of anode voltage and the corresponding Fowler-Nordheim data was analyzed.

The SEM images shown in Figure 75 show a completed device in a diode configuration. The CNTs, which are synthesized in a lateral orientation, grew selectively along the etched quartz sidewall. CNTs also appear along the edges of the metallic conductors, which is due to the resist walls acting as shadowing structures during the metal evaporation. This excess nanotube growth can be eliminated with another lithographic step which buries the exposed catalyst film; however it was not performed on the samples shown in Figure 76. It could easily be done during the
same lithographic step in which the gates are deposited. The distance from the CNT emitter tips to the anode is approximately 8 µm.

In Figure 77 a plot of the anode emission current as a function of the applied electric field is shown. The turn-on electric field will be defined as the electric field required to draw 1 nA of current through the anode. The laterally grown CNTs demonstrated a turn-on field of 1.4 V/µm. To calculate the current density, an estimate of the emitting area is necessary. Assuming the emitting area is comprised of the entire metalized sidewall, the dimensions of the original lithographic pattern can be used. The width of the emitting region is 25 µm and the height of the region is estimated at 15 µm. The estimate of 15 µm is reasonable since the angled evaporation was performed at 45° for a trench that was approximately 15 µm wide by 15 µm deep. As a result, the entire cathodic sidewall should be metalized down to the trench floor. From these values an emitting area of 3.75×10⁻⁶ cm² is calculated.
The I-V data in Figure 77 shows that the CNT emitters achieved a maximum current of approximately 3.0 µA at an applied field of 3.8 V/µm. Combining the maximum current with the estimate of the emitter area yields a maximum current density of 800 mA/cm². This value is considerably high, and may truly be higher since it is likely that the emission during the I-V testing originated from a smaller region than the estimated area. A turn-on field of 1.4 V/µm for the CNT emitters is in good agreement with the 1-2 V/µm range cited for vertically emitting geometries [142, 150-153] and is a significant improvement over other laterally emitting devices [20, 144], whose turn-on fields are often significantly higher than 1.4 V/µm.
Using the estimated emitting area, the corresponding Fowler-Nordheim (FN) plot is calculated and shown in the inset of Figure 77. To validate the electron transport as field emission, a linear fit of the data is performed and yields a straight line that is in good agreement with the experimental data. The linear fit is also used to estimate the electric field enhancement factor using Equation 11.

\[
\gamma = \frac{C \phi^{3/2}}{m} \rightarrow \gamma = \frac{(6.8309 \times 10^9)(4.5^{3/2})}{-2.5521 \times 10^7} \rightarrow \gamma = 2555
\]

Equation 22

Compared to earlier device designs, this particular geometry showed much higher performance. Though the calculated value for the field enhancement is high, it is important to note that it does contain some error due to the estimates made for the emitting area and the anode to cathode separation. Thus, it should not be treated as an absolute quantity. Additionally, the I-V data set shown and analyzed in Figure 77 is representative of the numerous other I-V sweeps performed on similar devices.

### 8.4.5 Thermal Testing

The temperature dependence of the device performance was investigated by placing a substrate heater under the device and resistively heating the sample while under vacuum. A thermocouple located near the device measured the temperature.
The experiment was done under high vacuum ($1 \times 10^{-6}$ torr) with the temperature ranging from 30 °C to 200 °C. Again, the device was operated in a diode configuration using the electrical test setup shown in Figure 78. To perform the experiment, the device was heated to the desired temperature and allowed to come to thermal equilibrium. Once the temperature was stable, I-V sweeps were performed. The resulting I-E curves at various temperatures were recorded and are shown in Figure 79. As can be seen from the data, the sample exhibits only a small change, that is not monotonic as a function of temperature, in emission characteristics.

Figure 78: Electrical setup used for the thermal testing of a device operating in a diode configuration. A resistive heater (not shown) is placed under the substrate to heat the device from room temperature to 200 °C.
It is clear that any effect of temperature on the device behavior is outweighed by other phenomena. Even at fixed temperature, the sample exhibits some variation in behavior from sweep to sweep. One potential explanation of this phenomenon involves the morphological changes to the CNT emitter surface due to the application of electric fields. It has been found that under low to moderate electric fields below the field emission threshold, the CNTs will flex to align themselves with the field. Upon removal of the electric field, the CNTs will revert back to their original orientation. However, under higher electric fields where relatively large field emission currents are extracted (100s of nA per CNT) the CNTs remain permanently deformed once the electric field is removed [154]. Since the maximum anode current extracted from the CNT array in this experiment is 500 nA (a relatively low total
current), it is expected that the CNT array will flex to varying degrees during each I-V sweep. Since electron field emission is highly dependent on the anode-cathode separation, any variation in the CNT flexing will introduce small variations in each I-V sweep, seen in Figure 79.

Another potential cause for the variance seen in Figure 79 is the temporal instability of the field emission from CNTs. This temporal instability has been reported by others [155] and can result in a 6% to 8% variance in emission current. Furthermore, the sample investigated was not subjected to any conditioning prior to data acquisition, and CNT emitters often require some “burn-in” before demonstrating stable behavior [156, 157]. It has been proposed that this is due to the presence of adsorbed gases that alter the effective work function [156, 157].

A final explanation for the emission variance is due to degradation of the CNTs during the subsequent I-V sweeps. The degradation occurs mainly as field evaporation of nanotubes due to the potentially high temperatures resulting from resistive heating along the nanotube [158, 159]. The resistive heating is exacerbated by defects in the nanotubes, and since the CNT emitters in the device are grown by thermal CVD, a technique known for high defect densities [62], degradation may be a cause for the emission variance.
Another effect on device performance that must be accounted for is the thermal expansion of the substrate materials. Since the emission characteristics are sensitive to small changes in anode-cathode separation, an estimate of this effect is necessary. More importantly, since the goal of this research is to create devices capable of high temperature operation, thermal expansion is inevitable. Thus, a drastic effect on device performance due to thermal expansion would prove especially problematic. Assuming a quartz substrate with a thermal expansion coefficient of $5.4 \times 10^{-7} \, ^\circ\text{C}^{-1}$ and a maximum operating temperature of 1000 °C the expected expansion would result in a 0.054% increase in all dimensions. For a 15 μm anode-cathode gap this translates to a 16.2 nm increase in separation. Comparing this to Figure 79 it is obvious that a change of 16.2 nm is negligible and should not appreciably contribute to variability in the emission. Though quartz was chosen as the substrate material for its high temperature stability, a calculation was necessary given the sensitivity of field emission to electrode separation.

The turn-on electric fields of 4 V/μm exhibited by this device also differ from a previously tested device, which had turn-on fields as low as 1.4 V/μm. This can be explained by the differences in the emitter morphology between the two devices. While it may be difficult to determine from SEM images, it is likely that given the random nature of the nanotubes synthesized by thermal CVD, the effect of nanotube-nanotube screening will differ greatly. This, coupled with temporal instabilities, emitter degradation, and electric field effects result in not only variance from sweep
to sweep, but from device to device. To achieve more uniform results the emitter morphology must be controlled more effectively and a burn-in process should be utilized to normalize emission characteristics.

Using the I-E data from Figure 79 and the same estimates for emitting area and electrode separation, Fowler-Nordheim plots were generated for each different temperature. The plot is shown in Figure 80.

Figure 80: Fowler-Nordheim plots and the corresponding linear fit from I-E data taken at a series of different temperatures. The device being tested was operated in a diode configuration under high vacuum.
The F-N data was analyzed and linear fits were completed on each data set corresponding to a device temperature. The resulting linear fits were in good agreement with the experimental data. The slopes of the lines, using Equation 11, were also used to calculate the electric field enhancement factors for the device at each temperature. Table 10 summarizes the results.

For each temperature, the electric field enhancement factor remained approximately constant, if not improving slightly as the temperature increased. The improvement could be attributed to desorption of molecules from the emitters, resulting in slight changes in the effective work function. Assuming the changes in the work function are small, this would likely have a minimal effect on the I-E characteristics.

Table 10: Estimates of the electric field enhancement factor taken over a range of different temperatures.

<table>
<thead>
<tr>
<th>Device Temperature (°C)</th>
<th>Slope from Linear Fit</th>
<th>Estimated Electric Field Enhancement Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>-6.7×10''</td>
<td>972</td>
</tr>
<tr>
<td>60</td>
<td>-7.5×10''</td>
<td>868</td>
</tr>
<tr>
<td>75</td>
<td>-6.8×10''</td>
<td>954</td>
</tr>
<tr>
<td>114</td>
<td>-6.7×10''</td>
<td>972</td>
</tr>
<tr>
<td>200</td>
<td>-6.4×10''</td>
<td>1015</td>
</tr>
</tbody>
</table>

Additionally, due to the estimates needed to calculate the enhancement factor, the slight changes to its value may be nothing more than the quality of the linear fit for each data set. Regardless, values of nearly 1000 for electric field enhancement are good, though improvements to the device (CNT morphology and alignment,
screening effects, etc.) can likely increase the enhancement even more with the end goal being an increase in device performance.

8.5 Third Generation Devices

8.5.1 Device Modifications

With the successful diode testing of the second generation of thermal CVD based devices, minor modifications were made to the fabrication process. The modification added a third lithographic step to the fabrication process that was able to pattern symmetric gates in three different orientations. The new mask was capable of placing the gates on the anodic sidewall (as drawn, Figure 81), the cathodic sidewall (dashed yellow rectangle, Figure 81), or both sidewalls to form a continuous conductor from the anodic to cathodic side of the trench. The general orientation of the electrodes was also changed so that the majority of the unwanted nanotubes produced by photoresist shadowing are eliminated. A schematic of the third device design is shown in Figure 81.

The fabrication process for the third generation of devices is practically identical to that of the second generation, with the exception of the additional lithographic step to pattern and deposit the gate electrodes. This process is performed in the exact same manner as the anode-cathode lithographic step by using a thick, negative resist followed by a lift-off. The metal is deposited by an angled evaporation technique done at 60° and is comprised of 300 nm of Ti. Once the gates are patterned the
fabrication process continues from the step shown in Figure 74D. The final modification made to the device was the creation of a separate photomask that varied the width of the trench. This was done to help avoid the potential shorting of the anode and cathode due to variations in the CVD growth process. As a result, when using this mask, the quartz RIE etch step duration increases such that the trench is as deep as it is wide (aspect ratio of 1). Currently, the trench width on the new mask is nominally 30 μm.

![Figure 81: Schematic representation of the current device fabricated using thermal chemical vapor deposition. (Left) Top-down view showing anode, cathode, gates, and CNTs. The dashed yellow rectangles indicate alternate gate locations. (Right) Cross-section of device concept showing the anode, cathode, and laterally grown CNTs (gates omitted for clarity).]

8.5.2 Diode Operation

Similar to the second generation devices, the third generation devices were first tested in a simple diode configuration. The electrical test setup was identical to that shown in Figure 78 and the initial tests attempted to explore the I-V characteristics of the new devices.

The I-V results for a typical device are shown in Figure 82. For this particular device, the width of the trench is still nominally 15 μm, and the emitting area and
anode to cathode spacing are $3.75 \times 10^{-10}$ m$^2$ and 8 μm respectively. The I-V plot of the data shows an exponential rise in the emission current as a function of increasing electric field. The device exhibits a turn-on field of 4.9 V/μm. This value, as expected, is in good agreement with the turn-on field of 4 V/μm exhibited by the results of Figure 79; however, it is not quite as robust as the 1.4 V/μm turn-on exhibited by the results of Figure 77. This may be attributed to differences in emitter morphologies. An improved CVD growth process producing more highly aligned and ordered CNTs would greatly improve the reproducibility from device to device.

The F-N plot was also constructed using estimates for the emitting area and the anode-cathode separation, $3.75 \times 10^{-10}$ m$^2$ and 8 μm respectively. The results of the plot are shown in the inset of Figure 82. A linear fit of the relevant data reveals a straight line that is in good agreement with the experimental data. Some spread in the data is seen, which can be attributed to instability of the field emission during the measurement. From the slope of the linear fit, the electric field enhancement may be estimated. Applying Equation 11 and incorporating the slope of the linear fit yields a value of 1505. While an improvement over the device used during the thermal testing, this value must be viewed with a degree of skepticism due to the spread of the F-N data and the lower than normal confidence in the linear fit. However, a result for the electric field enhancement above 1000 demonstrates good device performance.
Figure 82: I-V and F-N plots for a typical third generation thermal CVD based device tested in a diode configuration under high vacuum ($1 \times 10^{-6}$ torr).

### 8.5.3 Preliminary Triode Operation

After repeated success in testing the devices in a diode configuration, preliminary tests in a triode configuration were performed. The dimensions of the device along with the electrical test setup are shown in Figure 83.
Before attempting to operate the device in a triode configuration, diode emission (using only the Keithley 237 SMU) had to be verified in the device. This was performed in a similar manner as previous I-V sweeps. Once a viable device was found and the field emission verified, the gates were contacted electrically and the device was tested in a triode configuration. The electrical testing in a triode configuration was performed in high vacuum ($1 \times 10^{-6}$ torr). A Keithley 237 SMU was used to apply a constant current of 10 nA between the anode and cathode while also measuring the anode voltage required to generate such a current. A Keithley 2410 SMU was used to apply a potential to the gates while also measuring the gate current. To perform the experiment, the gate bias was ramped up from zero while simultaneously measuring the anode voltage and the gate current. The results of the experiment are shown in Figure 84.
In order to demonstrate triode operation, a potential applied to the gates must be capable of modulating the field emitted current between the anode and the cathode. In one configuration, a constant bias near the emission threshold is applied between the anode and cathode. The gate potential is then ramped up and the change in emission current is measured. In this electrical configuration an ideal result would show a small voltage change on the gates initiating a large change in current between the anode and cathode. This method was attempted using the aforementioned devices; however, it proved unsuccessful in limited trials. As a result, a constant current (rather than constant voltage) was applied between the anode and cathode. Thus, when the voltage on the gate was ramped up, changes in the anode voltage would indicate if any modulation to the emission was occurring. This constant
anode-cathode current proved more stable than the constant anode-cathode voltage, thus the triode tests were done in this manner.

To further analyze the plot of the anode voltage as a function of gate voltage, the behavior can be broken down into two separate regions. In Region 1, the device is field emitting with a constant current of 10 nA between the anode and cathode. It should also be noted that in this region, the gate voltage does not become large enough to have a significant effect on the anode voltage. It can be argued that as the boundary between Region 1 and Region 2 is approached (dashed line), some gate effectiveness is seen by the slight downward slope of the anode voltage. However, this may just be the result of the device undergoing a conditioning process which can have the effect of lowering the anode voltages necessary for emission. Since the effect of the gate voltage within Region 1 is likely minimal, it will be assumed that the behavior is primarily a result of electrically conditioning the device. The sudden large increases followed by equally sudden decreases in anode voltage are also indicative of this conditioning process and are evidently present in Region 1.

At the boundary between Region 1 and Region 2, which occurs at a gate voltage of 110 V, the effectiveness of the gate becomes evident. At this transition point, the anode voltage begins to decrease at a greater rate indicating the gate voltage is affecting the electric fields in the vicinity of the CNT emitters. As a result of this electric field modulation, the anode voltage required to draw a current of 10 nA is
reduced, thus a decrease in anode voltage is measured. As the gate voltage continues to increase, the anode voltage decreases in a linear fashion. However, the gate voltage cannot be increased arbitrarily. Given the geometry of the device, the gate electrodes are only a few microns farther away from the CNT emitters than the anode. As a result, once the gate voltage begins to exceed the anode voltage, a leakage current may appear on the gates. From the plot, this starts to occur at a gate voltage of 127 V corresponding to an anode voltage of 110 V. These results are in good agreement with the assertion that the gate voltage must usually equal or exceed the anode voltage before a leakage current is detected on the gates. As the gate voltage increases to 138 V, the magnitude of the leakage current on the gate rises to 10 nA, which is identical to the anode current. Further increases of the gate voltage simply result in larger currents through the gates, as shown in the plot.

Ideally, a field emission triode should be able to operate with an arbitrarily large gate bias without generating large leakage currents. Although the device being tested did not exhibit this ideal behavior, Region 2 does show some promising results. An expanded plot of Region 2 from Figure 84 is shown in Figure 85 with the addition of a linear fit of the anode voltage data. The slope of the linear fit yielded a value of -2, implying that within this region where the gate was effective, each 1 V increase in gate voltage would decrease the anode voltage by 2 V. However the most important observation is that a region exists where the gate current remains at its initial value (red dotted line) while the gate voltage is simultaneously modulating the emission.
This “operating region” represents the ideal characteristics of a triode where a gate voltage modulates the emission current while the leakage current through the gate is zero. The success shown by the presence of the “operating region” indicate that the chosen device geometry can demonstrate triode behavior, though further refinements and different device operating modes can likely lead to improved performance.

With the successful operation of the device, the next step is to look for ways of improving the results. Typically, field emission devices, similar to vacuum tubes and field effect transistors, can either be considered normally on or normally off, referring to the manner in which they are operated. In terms of field emission based devices, a normally “on” device has an anode-cathode bias that is sufficient to sustain electron transport via field emission for the desired application. A potential is then applied to the gate to reduce the electric fields and reduce or eliminate the emission current. Normally on devices have the advantage of very low gate leakage since the potential applied to the gate will repel electrons, thus they are easier to operate. This is particularly useful for digital electronics where low leakage is critical in device performance. The non-linear I-V behavior also enables large differences between the on and off states of the device. Analog electronics also benefit from the non-linear I-V behavior. Since a normally on device is operated at higher current densities requiring electric fields well above the emission threshold, the device is operating in a region where the slope of the I-V curve is very steep, an advantage in
analog electronics. As a result, any change to the electric field due to the gate will result in very large changes in emission current.

![Graph](image)

**Figure 85:** Plot of Region 2 from Figure 84 showing the anode voltage and gate current as a function of gate voltage.

Normally “off” devices are just the opposite. For this type of operation, an anode-cathode bias is applied such that it is just below the emission threshold (in some cases a little above it such that a small current is drawn). The gate potential is then used to turn the device on to the desired emission current, depending upon the application. These devices are more difficult to operate since the gate potential will attract electrons, thus making the possibility for high gate leakage a concern. As a result, much care must be taken with the geometry and fabrication of such devices.
Despite these problems, normally off devices are useful since they may facilitate more simplistic logic and computer architectures when used in conjunction with normally on devices.

For the results presented in Figure 84 and Figure 85, the device was operated as a normally off device since the application of the gate voltage had the effect of lowering the anode voltage, which is a similar measure of increasing emission current. It should be noted that operating the device as normally off likely sacrificed some performance. This is due to operating the device at the lower end of the I-V curve. In this region, despite the exponential I-V relationship, the slope of the curve is much less than that of a normally on device. As a result, changes in gate voltage are not as effective and do not produce extremely large changes in emission current, which is interpreted here by the behavior of the anode voltage. Further measurements operating the device as normally on may give a better representation as to the level of performance attainable from these devices. Additionally, measuring the anode current rather than the anode voltage will also provide more useful data for analysis.
9 Conclusions

Carbon nanotube based field emission devices in the form of diodes have been successfully fabricated. The devices were created using two separate CNT deposition techniques: dielectrophoresis and thermal CVD synthesis. Initial attempts to create a CNT based field emission device focused on using dielectrophoresis to physically deposit the CNTs at desired locations at the wafer level. The substrates were then processed using standard semiconductor techniques to complete the fabrication of the devices.

The resulting structures gave insight into not only the viability of CNT field emission devices based on the DEP technique, but also the underlying physics of the dielectrophoretic deposition process. DEP is a useful technique because it allows for a scalable method for manipulating and depositing CNTs using only electric fields. However, my results point to what may be a practical limit in the DEP process. My results suggest that the electrode dimensions and suspension density play a crucial role in CNT network reproducibility at the wafer level. Smaller electrodes have the disadvantage of a smaller interaction volume with the suspension, thus at low suspension densities, the potential for a given electrode pair to be unsuccessful in attracting a CNT increases. When the electrode size is increased, the interaction volume increases, and the effects due to low suspension density and random variations in local CNT density are averaged, leading to a more reproducible process.
Suspension densities must also be carefully chosen. At higher suspension densities, the CNTs agglomerate into bundles, which is often an undesirable result. To mitigate this problem, the CNT suspensions are horn sonicated and subsequently filtered to remove any large remaining bundles. However, unless the CNT density in the suspension can be increased significantly without a concomitant increase in CNT agglomeration, wafer-scale fabrication of CNT devices may be limited to those devices where the electrodes interact with a sufficiently large volume of suspension.

The results of the DEP tests also produced the development of an in-situ monitoring technique by which the DEP network current is measured as a function of time. Due to the reproducibility of this current-time curve it was concluded that this method was an adequate method to determine CNT deposition progress, and to also determine the appropriate end points for the process. The development of this new technique, along with the correlation to the deposition progression, presents the possibility of a closed loop feedback system for large scale fabrication.

The DEP based devices, though successfully fabricated, proved to be a challenge to operate. Numerous modifications to the fabrication process were required to create a testable device. The few electrical results generated by the DEP devices also exhibited lower than expected performance. Low maximum currents, reduced yield due to contamination and fabrication issues, large operating voltages, and low electric field enhancement hindered high performance operation. Overall, the devices
suffered from numerous technical hurdles. Perhaps the principal issue was the cleanliness of the CNT emitters. Since the DEP process deposits the CNTs as one of the initial steps, the CNTs are exposed to the remainder of the fabrication process. Measures were taken to help protect the CNTs; however, the success of these measures remains uncertain in terms of electrical behavior. Examination via SEM showed visual evidence that the CNTs were cleaner; however, the difference was not measured electrically. Many of the other issues with the DEP devices involved fabrication steps, with the CNT cantilevering step being the most difficult. Due to the inability to create a uniform emitter edge via RIE, the device inevitably suffered from emission non-uniformities. In addition, the yield of viable devices would be reduced since the optimal cantilevering etch would differ for each device.

Though the electrical results for the DEP based devices were not as expected, the development of the DEP devices would eventually lead to a much more promising device design. Additionally, the discoveries made using dielectrophoresis provide a useful tool to create highly reproducible CNT networks on a large scale. Such potential applications would include CNT sensors, device interconnects, optical gratings, among many others. However, as a method for creating a lateral field emission based device, DEP remains a challenge.

Upon reaching this conclusion, it was determined that a radically new device design was necessary that utilized a different method for creating the CNT emitter structure.
After design modifications, a device based on a thermal CVD synthesis of the CNT emitter structure from an etched quartz sidewall was developed. In this design, the CNT emitters are synthesized during the final fabrication step forming an array of clean, robust emitters. They do not suffer from fabrication induced contamination, and are free from amorphous carbon due to the cleanliness of the thermal CVD process. These devices were successfully fabricated and tested as both diodes and triodes. Electrically, this new device could transport high currents, exhibited low operating voltages, and showed high electric field enhancement at the emitters. Thermal tests were also performed on the device in a diode configuration over a temperature range from 30°C to 200 °C without a change in device performance, thus validating the claim of temperature independent operation. Triode operation was also performed. The device exhibited an operating region where the gate voltage modulated the emission current without any leakage current to the gate. Although the leakage current did rise eventually, this first attempt at triode operation proved successful. Further work is currently underway to improve the electrical and thermal performance of the triodes.

While trying to produce a device with superior performance to those currently available, I realize that the CNT field emission devices will most likely be used for niche applications, particularly harsh environments. Currently semiconductor technology, while incredibly useful in everyday life, is not able to function at high temperatures or in the presence of ionizing radiation. There are two solutions for
solving this problem: either adequately cool or shield the device from the harsh environments, or create a device that is unaffected by temperature and radiation. The former solution has been employed for the most part; however it can become expensive and impractical to provide the necessary cooling or radiation shielding, especially in space applications where weight directly translates to increased costs. It has been our goal to achieve the latter.

These devices have characteristics that could result in benefits to an exceedingly wide range of applications. High-frequency analog applications are particularly of interest because of the very low capacitances and the high current/unit area capability of typical CNT field emitters, which is in the Amps/cm² range. Also, since field-emitted current rises exponentially with increasing applied electric field, these devices have the potential for large gain as well; however, the harsh environment niche is where I see the CNT field emission devices as a solution to the current problem. The devices provide the basic building blocks (diodes and triodes) for modern electronic devices while offering unaffected performance at high temperatures and in the presence of ionizing radiation. Neither poses an issue for proper device functionality since the radiation will not generate electron-hole pairs as no semiconductors are present. Additionally, the method of electron transport is Fowler-Nordheim tunneling, which is also independent of temperature as well as radiation. I believe that the fabrication of CNT field emission devices will lead to
better suited electronics for use in harsh environments and space exploration, and may even find everyday uses in both commercial and military electronic devices.
References


