NANOSCALE GAS SENSORS AND THEIR DETECTION MECHANISMS: CARBON NANOTUBES AND BEYOND

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By

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The research presented in this thesis focuses on the experimental investigation of nanoscale electronic devices for gas sensing applications. The majority of the experiments were conducted on carbon nanotube field-effect transistors (CNTFETs) made with variable density carbon nanotube networks. The carbon nanotube networks were grown using chemical vapor deposition on doped silicon wafers capped with silicon dioxide. Contact electrodes were attached to the networks with standard e-beam lithography and thin film deposition techniques. To better understand the sensing mechanism of CNTFETs, numerous samples were fabricated with varying densities of nanotubes and nanotube junctions. These samples were exposed to nitrogen dioxide and the change in conductance was recorded. Selected parts of the device were then passivated with a thick photoresist to determine whether they contribute to the sensing mechanism.

Our previous work showed that for devices made with a single CNT, the response to nitrogen dioxide was mainly due to modifications at the contact interfaces rather than molecular adsorption on the nanotube sidewalls. However, here we show that when using CNT networks, both gas sensing mechanisms are involved. We will illustrate this through the comparison of the experimental response of high-density versus low-density CNT networks and show that the effect of adsorption is linked to the number of CNT junctions, or cross-over points, in the
network. Adsorption plays a major role for high-density networks. Its effect is much weaker for low-density networks and not measureable in a single nanotube, where the response is mainly due to the electrodes.

Experiments were also performed on field-effect transistor devices with molybdenum disulfide (MoS$_2$) being substituted for the nanotubes. These devices were fabricated using the same substrates and metal deposition techniques used for carbon nanotube devices; however the MoS$_2$ was mechanically exfoliated onto the wafers. Their gas sensing properties and majority carrier mobilities were explored. While testing these devices, we found that the choice of metals used for electrodes had a great impact on device behavior. In addition to their gas sensing properties, the potential use for optoelectronics was studied.
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INTRODUCTION

Today’s world is increasingly dominated by electronic devices which continue to shrink in size while expanding their capabilities. However, several challenges in the miniaturization of silicon technology, including design complexity and heating due to power dissipation, have sparked the search for new electronic materials with reduced dimensions.

Carbon nanotubes (CNTs), a carbon allotrope, are hollow cylinders of carbon atoms. They are one dimensional (1D) conductors that can be either metallic or semiconducting depending on chirality. They are widely studied for their electrical and mechanical properties, and single-walled carbon nanotubes (SWNT) can have diameters smaller than one nanometer. CNTs are ideal for integration into many different common micro- and nanoelectronic devices because of their small size and high conductivity.

Since their discovery over two decades ago, a flurry of theoretical and experimental work investigated their properties for applications as field effect transistors, memory devices, and gas sensors. [1] This work will focus on CNT gas sensing properties. Gas sensing was first reported for SWNTs used as the conducting channel of a field effect transistor (FET). [2] CNT-based sensors possess many factors that make them attractive alternatives to other commercial gas sensors. They operate well at room temperature and in air. [1-4] They have a low detection limit, in the parts per billion (ppb) range that makes them extremely sensitive. [1-7] Finally, these sensors operate at a low current threshold, which translates into small power consumption. [4]

Questions remain about the nature of the sensing mechanisms. There are two main possible mechanisms: charge-transfer due to the physical adsorption of gas molecules onto the CNT
sidewall and the modulation of the Schottky barrier between the CNT and metal electrode contact.

Our research group previously made devices with a single CNT and covered the contact electrodes with a protective layer, leaving most of the CNT surfaces exposed. These experiments demonstrated that, in a single CNT device, Schottky barrier modulation at the interfaces between the CNT and the contact electrodes is the main detection mechanism for NO\textsubscript{2}. [3] However, the detection mechanism for CNT network devices was still unclear.

Here I investigate CNT networks with a similar contact passivation technique. By studying networks with different densities, I find that although no effects of gas adsorption on single tubes can be measured, CNT-CNT junctions contribute to the network device response. Gas adsorbed on the junctions changes their conductance via charge-transfer thereby changing the conductance of the whole device.

Another material that can be reduced to nanoscale dimensions is molybdenum disulfide (MoS\textsubscript{2}), a transition-metal dichalogenide semiconductor that been used as a lubricant for many years. [8, 9] The MoS\textsubscript{2} crystal cleaves at the atomic planes which allows for single layers to be deposited onto substrates. A single layer of MoS\textsubscript{2} consists of two hexagonal lattices of sulfur atoms which sandwich a hexagonal lattice of molybdenum atoms. MoS\textsubscript{2} is a promising material for integration into FETs due to its very good mobility and temperature stability. Other potential applications investigated in this work are photovoltaic devices and gas sensors.

This thesis is structured as follows: Chapter 1 provides an overview of CNT and MoS\textsubscript{2} structure and electronic properties, and an introduction to gas sensing; Chapter 2 contains a full description of CNT gas sensor design, fabrication techniques, and measurement set up; Chapter 3
presents the experimental results of the measurements of CNT network sensors, and Chapter 4 focuses on the MoS$_2$ experiments. This chapter includes the description of several different fabrication techniques and the results of the measurements of gas sensing, mobility, and the photovoltaic effect seen in MoS$_2$ devices.
Chapter 1

Background

One of the core tenets of modern electronics is Moore’s Law. Moore’s law effectively states that the number of transistors in a computer processor will double every two years. While this law has held for several decades, the rate of increase has begun to slow due to the limitations of conventional materials like silicon. However, new materials like CNTs and molybdenum disulfide offer scientists alternative ways to create nanometer scale channels for transistors. These transistors can be integrated into a wide array of devices for gas sensing and optoelectronics. Devices made with nanometer scale materials hopefully will allow Moore’s law to continue to apply and improvements to continue in device performance.

1.1 Structure of Carbon Nanotubes

In the past twenty years, few scientific advancements have produced as much research activity as the discovery of carbon nanotubes. Since 1991 countless studies on CNTs and their uses have been published and many billions of dollars have been spent in the process. CNTs have roots in the breakthrough of buckminsterfullerene, more commonly known as a buckyball \( \text{C}_{60} \), and other fullerenes in the mid-1980s. CNTs, which are a part of the fullerene family, are one of carbon’s allotropes. The rich chemistry of carbon means it is the basis of thousands of materials with a large range of properties owning to carbon’s ability to form different types of chemical bonds from the 4 valence electrons in N=2 electronic levels. [1,10]
The hybridization of the 2s and 2p orbitals gives way to sp, sp$^2$, and sp$^3$ orbitals. A sp hybrid orbital is a combination of the 2s orbital and one of the 2p orbitals. (See figure 1-1) To minimize electron density and energy, sp orbitals force molecules into linear shapes. The sp$^2$ and sp$^3$ hybrid orbitals combine one 2s orbital and two 2p or three 2p orbitals respectively. The sp$^2$ orbitals cause molecules to form a trigonal planar geometry. Carbon based molecules such as ethane use sp$^3$ orbitals where all four bonds are occupied by hydrogen atoms which form a tetrahedral arrangement to minimize electron repulsion.

![Figure 1-1](image)

**Figure 1-1.** a) s and p$_x$ orbitals and their combination into a sp hybrid. b) s and p$_y$ orbital and their combination into a sp hybrid

Graphite is a layered structure made of weakly coupled sheets of carbon atoms. A single layer of graphite is called graphene. For each carbon atom in graphene, three valence electrons occupy sp$^2$ hybrid orbitals and form bonds in a hexagonal lattice structure with the sp$^2$ electrons of three neighboring carbon atoms. For each atom, the 4$^{th}$ valence electron is free and occupies a p$_z$ orbital. Therefore, two types of bonding can occur with graphene, the sp$^2$ orbitals form $\sigma$
bonds and the \( p_z \) orbitals can form \( \pi \) bonds, seen in figure 1-2. [1,10] Carbon-carbon covalent bonds are what give carbon nanotubes their mechanical strength. [11]

**Figure 1-2.** Shows a) \( sp^2 \) hybrid, b) \( \sigma \) bonding of \( sp \) orbitals, and c) \( \pi \) bonding of \( p \) orbitals

A graphene layer rolled in a shape of a cylinder forms a single walled carbon nanotube (SWNT). For multi-walled nanotubes, several concentric layers of graphene are rolled around each other. The wrapping of a sheet can be represented by a chiral vector \( C_h = n\mathbf{a}_1 + m\mathbf{a}_2 \), where \( \mathbf{a}_1 \) and \( \mathbf{a}_2 \) are the primitive vectors of the graphene crystal lattice. (See figure 1-3) [1]
A nanotube with chirality $C_h$ can be obtained by rolling the sheet in such a way that the end of the vector $C_h$ is folded onto its tail. Moreover, the chirality vector also determines the diameter, $C_h = \pi d_{CNT}$, where $d_{CNT}$ is the nanotube’s diameter. [11,12]

The components of the chiral vector, $n$ and $m$, are used as indices to determine the CNT chirality (figure 1-3). We distinguish two special CNT types. “Armchair” nanotubes correspond to indices with $n = m$, whereas $m = 0$ indicates “zigzag” CNTs. These names are by no means random. They draw their origins from the shape of the cross section of the CNTs, as shown in figure 1-4.

Figure 1-3. Chiral Vectors on a CNT lattice
The zigzag tube is easiest to understand as the bonds zig and zag up and down. The armchair configuration requires some imagination. The two outer flats represent the armrests and the center flat is the seat. When neither of these conditions is met, the CNT is considered to be chiral. This wrapping also determines if the CNT is metallic or semiconducting. Metallic CNTs occur when $n - m$ is a multiple of 3, including the armchair configuration. [1, 10] When a CNT does not meet this condition, it is generally semiconducting in nature. This rule means that roughly two thirds of CNTs are semiconducting and one third are metallic. [1, 10, 11]

The relation between the chirality and electronic properties (metallic or semiconducting) can be understood considering that the Brillouin zone of graphene has six corners with only two non-equivalent points, indicated as K and K’ in figure 1-5, originating from the two carbon atoms in the real space lattice. [1, 10]
The electronic structure of graphene determines the electronic structure of the SWNTs, after applying the periodic boundary condition that reflects the cylindrical shape of the tube. [1,10] We define the components of the wave vector \( \mathbf{k} \) as \( k_{\perp} \) and \( k_{\parallel} \), where \( k_{\perp} \) is the component along the circumference of the SWNT and \( k_{\parallel} \) follows the axis of the CNT. [1, 10] Using periodic boundary conditions, it is possible to express the quantitization of the \( k_{\perp} \) as \( C_n k_{\perp} = 2\pi n \) where \( n \) is an integer [1, 10-12] Whereas we assume that \( k_{\parallel} \) varies continuously, as the tube can be viewed as being infinitely long. [1, 10]

Tight binding calculations show that the dispersion relation near the Fermi energy has a conic shape at the six \( K \) points for the valence and conduction bands. [1, 10, 13] This is key to determining the electronic structure of the CNT. The few allowed values of \( k_{\perp} \) restrict the band structure into one dimensional (1D) subbands. [1, 13]
In fact, the allowed values of $k_{\perp}$ identify vertical planes in the $E$ vs. $k$ plot that cut the cones into 1D subbands and determine the electronic transport characteristic of the CNT. If the plane goes through a K point, there is no gap between the 1D conduction and valence subbands. Therefore a metallic nanotube is created. If the plane does not intersect the K point, a semiconducting tube is created. [1] This concept has been illustrated in figure 1-7.
Thus the chirality vector and diameter of SWNTs govern the CNT dispersion relation. For every CNT, there are two subbands close to the Fermi energy, for the K and K’ points respectively.

CNTs show remarkable physical and electronic characteristics. Single-walled CNTs have been shown to be ballistic 1D conductors, namely the electronic mean free path is larger than the length of the conductor. [11, 14] However, the two-terminal conductance of CNTs is not infinite. This is because the number of conducting channels in these 1D structures is very small. The Laundauer formula shows that the conductance of a 1D ballistic conductor is given by

\[ G = \left( \frac{2e^2}{h} \right) \sum_i T_i \]

where \( 2e^2/h \) is the quantum conductance (accounting for spin degeneracy), \( T_i \) is the transmission of a conduction channel and \( N \) is the number of channels. For a metallic or a semiconducting nanotube, there are two degenerate channels for energies close to the Fermi energy, corresponding to the K and K’ subbands, therefore the resistance in the absence of scattering and with ideal contacts (\( T_i = 1 \)) is \( h/4e^2 \approx 6.5 \text{ kΩ} \). [11, 14] The primary causes of

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**Figure 1-7.** Dispersion relation cross-section and graphic band structure of a) metallic SWNT and b) semiconducting SWNT
Adapted from [35]
resistance in CNT devices, in addition to the contacts, are defects in the CNT itself and phonon scattering. [11, 14]

As discussed above, there are two main types of SWNTs: metallic and semiconducting. Metallic tubes do not have a bandgap and their conductance is not greatly affected by chemical or electrical doping, therefore we focus on semiconducting nanotubes for application as gas sensors.

1.1.2 Device

Field Effect Transistor

One of the breakthroughs of modern electronics is the transistor. Since its creation at Bell Laboratories in the late 1940s, it has been used for countless applications and has been the subject of intense study to increasingly improve its characteristics. [15] A transistor can be used to switch or amplify electronic signals and has been developed into many different types. Here the focus is on the Field Effect Transistor (FET). A FET is a device with three terminals: normally a source electrode, a drain electrode, and a gate electrode. [16] These parts’ names also describe their function. The gate electrode’s main function can be likened to a faucet; it opens and closes the electrical current channel between the source and drain electrodes thus allowing or hindering the flow of current in that channel. The gate electrode’s voltage ($V_G$) produces an electric field and the electric field modifies the channel’s resistance which will in effect turn the device off and on. When the $V_G$ exceeds the threshold voltage ($V_{th}$), the transistor is turned on and current will flow. [15, 16] Depending on the device, the primary charge carriers can be either electrons ($n$-type) or holes ($p$-type), meaning that change carriers contributing to transport are primarily in the conduction band or in the valence band respectively.
One of the most common FETs in modern electronic devices is the Metal Oxide Semiconductor FET or MOSFET. In industry, the semiconductor of choice for MOSFETs is silicon. MOSFET fabrication is based on established techniques that have been refined to improve performance during the past 50-plus years. Silicon micro-machining through dry and wet etching as well as photolithography are the back bone of the MOSFET industry. Figure 1-8 shows a $p$-type MOSFET. It is a $p$-type device since the small doped regions in figure 1-8 are $p$-type and the channel that will be formed is also $p$-type. Those small regions are implanted with a dopant, such as boron, into an overall $n$-type wafer. If the doping of the Si substrate and the smaller regions were reversed, it would be an $n$-type MOSFET.

![Figure 1-8. An example of a MOSFET device.](image)

The $V_G$ controls the current in a MOSFET by controlling the size of the conducting channel. Miniaturization of MOSFETs is becoming increasingly difficult. The channel has been reduced to about 10 nm, approaching the depletion length, therefore the channel disappears when this
scaling limit is reached. Moreover, the heat caused by the current flow becomes another issue to deal with at such a small scale. The heat must be dissipated to avoid destroying the device.

In 1998, SWNTs were integrated into a FET, creating the first CNTFET and providing a novel approach to transistor fabrication. [1] In a CNTFET, a semiconducting carbon nanotube is the conducting channel between the source and drain electrode. The CNT has many favorable electronic properties which makes it ideal for integration into FETs. CNTs can act as 1D conduction channels, their transport can be ballistic, and they can carry very large amounts of current. [1, 10]

Semiconducting CNTFETs work in similar fashion to normal FETs and MOSFETs. At zero gate voltage, the Fermi energies of source and drain electrodes are aligned within the CNT gap, thus allowing no current to flow. A positive $V_G$ applied to the device lowers the energy of the electrons in the CNT. Therefore for a sufficiently high $V_G$, the Fermi energies ($E_F$) of the source or drain electrode will be aligned with the bottom of the conduction band. Any current in this

![Figure 1-9. a) CNTFET device where the Si substrate acts as the gate electrode. b) Energy band diagram for a CNFET](image)
regime is n-type. On the other hand, a negative $V_{GS}$ shifts electronic energy levels upwards and the device turns on when $E_F$ of source and drain is aligned with the edge of the valence band. This produces $p$-type conduction since holes are the dominant carrier. (See figure 1-10)

The simplified model is complicated by the presence of Schottky barriers and band bending phenomena.

Schottky Barriers (SB) typically form at an interface between a metal and a semiconductor (MS). Metals are conductors with no band gaps. The Fermi level of the metal
$E_{Fm}$ and the Fermi level of the semiconductor $E_F$, equilibrate via charge transfer from the material with the higher Fermi energy to the material with the lower Fermi energy. The electrostatic potential due to the charge transfer causes the energy bands to bend. [16] This remains true for a metal CNT (M-CNT) interface.

![Diagram](image)

**Figure 1-11.** Schottky junction between a) a metal and a CNT where $\Phi_m > \Phi_{cnt}$ and b) a metal and a CNT where $\Phi_m < \Phi_{cnt}$

The work function of the metal, $\Phi_m$, is the minimum energy required to remove an electron from the metal. Therefore, it is the difference in energy between the Fermi energy and the vacuum level, where the electron is free. The work function is defined the same way also for a semiconductor where the Fermi energy lies in the band gap. The height of the Schottky barrier ($\Phi_{SB}$) is defined as the difference between the $E_{Fm}$ and the majority carrier band edge of the semiconducting CNT at the M-CNT interface. For the most generic case, a $n$-type barrier, the SB
height is the difference between the $E_{Fm}$ and the conduction band minimum. (figure 1-11a) On the other hand, if the SB was $p$-type SB, the SB height is the difference between the valence band edge and $E_{Fm}$. (figure 1-11b)

Electrons fill the energy levels up to the $E_{Fm}$ in the metal, but there are no electrons at the $E_{Fcnt}$ since it lies inside the band gap. Despite this, the work function of the semiconducting carbon nanotube $\Phi_{cnt}$, still corresponds to the minimum energy needed to remove an electron and it is different from the electron affinity, shown in figure 1-11a. Assuming that $\Phi_m$ is greater than $\Phi_{cnt}$, when the M-CNT interface is formed, the electrons in the CNT transfer into the metal. This causes an accumulation of electrons near the surface of the metal. As more electrons tunnel into the metal, a depletion region is also formed in the CNT with width $W$. The process continues until the Fermi energies are aligned. A built-in potential, $V_0$, forms near the MS interface and the energy bands of the semiconductor bend. Bending does not change the properties of the rest of the semiconductor, which is far away from the interface.

The quantity $\Phi_m - \Phi_{cnt}$ is the energy required to move one electron from the semiconductor to the metal. To move an electron in the opposite direction, to the conduction band of the semiconductor, the potential barrier height is given by the Schottky Barrier height (SBH), $\Phi_B$.

$$\Phi_B = \Phi_m - \Phi_{cnt} + \frac{E_g}{2} = \Phi_m - \chi = eV_0 + (E_c - E_{Fcnt})$$  \hspace{1cm} (1)

On the other hand, if $\Phi_m$ is less than $\Phi_{cnt}$, the Fermi energy of the metal, $E_{Fm}$, will be higher than the Fermi energy of the CNT. A depletion region will still form at the M-CNT interface due to charge transfer and the Fermi energies align. The bands will still bend but in the
opposite direction, figure 1-11b. In this case, the SBH is the difference in energies of the valence band maximum (VBM) and the Fermi level of the metal $E_{Fm}$.

The Schottky barriers in a device are not always the same for the conduction band and the valence band. This difference causes the $I_{SD}-V_G$ curves to have asymmetric behavior, see figure 1-10. The position of the Fermi level of the tube and the equilibration of the Fermi levels after contact with the metal affect the barriers. The asymmetry is easily seen in figure 1-10, since the saturated p-type current is higher than the n-type current. Saturation occurs when the gate voltage pulls the bands up (p-type) or down (n-type) to the point where the barrier is very thin. When the barrier thins, it becomes much easier for the majority carriers to tunnel through it.

1.1.3 Device Characterization

**Hysteresis**

Another important characteristic of CNT transistors is hysteresis. Hysteresis can be defined as the lagging of a physical effect on a body behind its cause. This manifests itself during electronic characterization of devices. When an $I_{SD}$ vs. $V_G$ measurement is taken by sweeping $V_G$ continuously within a fixed range, the current level does not follow the same path throughout the measurement. Figure 1-12 demonstrates that, as the gate voltage $V_G$ sweeps through its cycle, the $I_{SD}$ vs. $V_G$ produces a hysteresis loop.
The red arrows in figure 1-12 show the counter clockwise orientation of the loop. This loops starts at $V_G = 0$, the voltage sweeps to -10V, then sweeps back through zero to +10V.

As mentioned earlier, the current in a FET is modulated by shifting the Fermi energy into the valence and conduction bands with an electric field. While the exact cause of hysteresis can be debated, its origin is the shielding and enhancement of the effective electric field on a FET channel. In a MOSFET, traps in the insulating layer between the gate and channel modify the local electric field felt by charge carriers with respect to the field applied by a gate voltage. [15-17] For a CNTFET, there are several suggested causes of hysteresis. Since CNTFETs have
similar architecture, charge traps in the oxide are one possible cause. [17] Another possible charge trap location lies in the thin water layer that forms on top of the CNT and the SiO$_2$ layer.[17-19] Heating the devices reduces the size of the hysteresis loop by releasing the water layer. [19] Additionally, charges can be trapped in the SiOH groups (silanol) at the top of the SiO$_2$ layer. [17, 20]

**Selective Electrical Breakdown**

A CNTFET can also be built using multiple CNTs connected in a network rather than single CNTs. Due to the lack of control of what types of CNTs are grown, most networks are a mix of both metallic and semiconducting tubes. This mix causes the devices to have less than ideal transfer characteristics. Selective electrical breakdown (SEB) is an incredibly useful technique that physically modifies the CNT network and is applicable to devices with either SWNTs or MWNTs. [21, 22] When CNTs are mixed in a network, the I$_{SD}$ vs. V$_G$ will show both metallic and semiconducting nanotubes contributing to the conductance, since they are connected in parallel.
This is evident in figure 1-13 where the current in the device cannot be turned off, due to the persistent background current carried by the metallic nanotubes in the range of $V_G$ where the semiconducting tubes are off. This produces devices with characteristics that are not ideal for application as a gas sensor because metallic carbon nanotubes are less sensitive to gases compared to semiconducting tubes. The metallic component must be removed to produce a device with good semiconducting characteristics. [3]

The process of SEB, which is applicable to both MWNTs and SWNTs, was pioneered over 10 years ago at IBM. [21] The process involves increasing the amount of current through the metallic CNTs until they break down while the semiconducting tubes stay intact because they are biased in the off state. SEB uses a FET’s gate electrode to turn the CNTs on or off. When $V_G >> 0$, electron conduction dominates, thus $n$-type tubes carry the current and are in the on state.
Conversely, $p$-type tubes are in the off state and carry almost no current. Metallic tubes are unaffected by the gate potential and are always on.

To burn off the metallic tubes, instead of sweeping $V_G$ and keeping $I_{SD}$ static, the method is reversed. The $V_G$ remains static and the $V_{SD}$ is increased to a large positive value, increasing the $I_{SD}$ through the device. The $V_G$ is chosen to maximize the number of semiconducting tubes in the off state, corresponding to the minimum $I_{SD}$. At fixed $V_G$, the increasing $I_{SD}$ heats the metallic tubes furthering breakdown. Taking a device from a curve such as figure 1-13 to one that mimics a full semiconducting CNT can take several cycles of SEB. Each cycle sweeps the $V_{SD}$ to larger positive values than the last cycle. In between sweeps, an $I_{SD}$ vs. $V_G$ measurement is taken for comparative purposes. The cycles end after the device demonstrates a high quality transfer curve, or the device is accidently destroyed.

In the case of MWNTs, the current will obliterate the outermost shells in MWNTs and continue to destroy subsequent shells until completely turned off, leading to quantitized drops or steps in the current. [21, 22] Analogously, SWNTs are destroyed one by one until the total current drops to zero.
Bundles, ropes, or networks of SWNTs behave like a combination of MWNTs and single SWNTs. The current initially drops in steps until only a few or a single tube carries the current and then breaks down. Ropes of SWNTs thin as the outermost SWNTs are destroyed. [21] Bundles or networks react differently. Breaks will occur in preferential spots such as defect sites and where SWNTs cross. [23]

Oxidation is the main mechanism of tube destruction during SEB. This oxidation typically occurs in three places along the CNT. The first is a defect site. The second location is where the tube bends due the substrate itself or, in the case of the networks, where other nanotubes are underneath it. These high curvature points are where the carbon bonds are stressed and deformed making them similar to a defect site. The final position where breakage occurs is the geometric middle of a tube, which is the halfway point between the two electrodes.

Figure 1-14. Network device with full SEB (all nanotubes are burned off), red dashed line is $I_{SD}=0$. 

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The reason for breakage occurring at the tube’s middle is joule heating. [24-26] The middle of the SWNT breaks because the metal contacts at the ends of the CNT act as heat sinks. [24-26] The heat sinks absorb the heat from the nanotube and thus keep those areas at a lower temperature.

SWNTs typically breakdown at roughly 600°C, for normal atmospheric conditions, but the breakdown temperature (T_{BD}) increases in vacuum with the absence of oxygen. [25]

1.1.4 Device Application

Gas Sensors

Gas sensors are an integral part of everyday life, not just in industry but in most homes as well. Carbon monoxide is a perfect example of a gas that can be harmful. Detectors for this gas can be found in many mass market retailers across the country. Another harmful gas is radon which is a radioactive gas that can cause lung cancer. [27] The federal government, namely the Environmental Protection Agency, warns the general public about how to test for, and mitigate the possible effects of radon. [27] For these reasons, cheap, sensitive, and reliable gas sensors are always in need and always being developed and refined.

In industrial settings such as bus and truck repair facilities and warehouses, nitrogen dioxide (NO_{2}) is a harmful gas that can accumulate and cause damage to humans. NO_{2} irritates the lungs and mucous membranes of the mouth, nose, and eyes. [28] Moreover, it is a by-product of fires and diesel exhaust. [28, 29] For these reasons, the Center for Disease Control has helped impose a federal exposure limit of 1 part per million (ppm) over long periods, over 24 hours, and 5ppm short term. These exposure limits are very low and dictate the requirement for very sensitive sensors.
Many companies produce several different types of gas detectors in various form factors and detection methods. One of the simpler detectors is a gas detector tube. This is a glass tube, roughly a few inches long, which comes in two different types, diffusion and pump aided. Diffusion tubes are passive detectors. They are carried on a worker’s person all day long. Pump aided tubes are placed in a pump and the air is sampled at a specific time. Both tubes work on the same principle of operation, as the ambient atmosphere passes through the tube, chemicals in the tube react with a target molecule and cause the contents of the tube to change color. As the concentration of the gas increases or over all exposure accumulates, the more intense the color change. The process is simple, effective, and relatively cheap.

Depending on the target gas, sensitivity, manufacturer, and type of tube, prices range from $34 to $79 per box of 10. Moreover, these tubes have a high degree of sensitivity. They can detect concentrations as low as 0.5 ppm and as high as 200 ppm, ranges designed to stay within those set by the government. One of the main drawbacks to these products is their disposability.

Other sensors including electronic products offered by companies such as Honeywell are the size of a digital multimeter. These devices generally have a replaceable resistive thin film sensor which is attached to an electronics package. This package measures the output of the sensor and translates it to the display for real time measurement. These do have an advantage over the tubes since they include alarms to warn the user. Their working lifetimes are limited by batteries, which can last 24 months, and by the normal lifetime of general electronics. Moreover, they are much more durable as they are made of thick plastics instead of a thin glass tube. The detection limits and sensitivities of these sensors varies by manufacturer and
they range from 0-20ppm or 0-100ppm, with resolutions down to 0.1ppm. [31] Finally, they can log the data for display and later analysis.

Several manufacturers make similar products which vary in price from ≈$400 to over $700. [32] Honeywell’s detector is sold for slightly less than $500. The prices can be prohibitive for some users. Moreover, since they are single-gas detectors, which is good for some specific applications, several single-gas detectors must be purchased and operated simultaneously in environments where more than one harmful gas may be present.

Once carbon nanotubes were successfully integrated into field effect transistors, one of the first real world applications tested and published was the gas sensor. [2] CNT-based sensors show great promise as a possible alternative or replacement for products currently on the market. Many factors make them attractive. One of the most important is the ability to function in ambient conditions i.e. at room temperature and in air. [2-4] This is particularly important since a sensor that cannot detect a target gas due to sensitivity to other atmospheric gases, such as nitrogen, is useless. Another important factor is compatibility with CMOS technology. [2-4] Standard silicon based CMOS fabrication techniques have been adapted to create CNT sensors. [2-4, 15] There are numerous silicon device manufacturers that already invested substantial sums on existing production facilities to produce CNT gas sensors. [33] Integrating CNTs into current fabrication production without a major retool lowers the start up costs and makes them an ideal candidate for business expansion or extension.

Moreover, CNT gas sensors can operate at low current thresholds which allow for small power consumption. [4] Businesses are always seeking methods to cut expenses and as the costs of energy continue to climb, any way to reduce energy consumption will draw great amounts of
interest. Energy costs can be a large part of a business’ overhead and reducing it increases profits. CNT sensors are also very attractive for their sensitivity to several gases, extremely low detection limit (ppb range), and room temperature operation. [2, 4-7]

Due to all these advantages listed above, gas sensing properties of CNTs have been widely studied in the past 13 years. [2-4] Yet to this day, there are open questions about the sensing mechanism. The two main possible mechanisms are charge transfer due to the physical adsorption of gas molecules onto the CNT sidewall, and the modulation of the Schottky barrier between the CNT and metal electrode contact.

The work function of a metal is the energy needed to remove an electron. Gases can induce changes in the work function of metals. When NO₂ interacts with a metal, it will withdraw electrons and will change the surface charge on the metal. This change in charge will create an electric dipole at the surface which generates a small electric field. That electric field affects the amount of energy needed to remove an electron. This change in work function will in turn change the shape of the Schottky barrier and the SBH. The SBH at the contacts influence the conductance of the device.

Our previous work on devices made with a single CNT and contacts covered by a protective layer, leaving most of the CNT surface exposed, demonstrated that Schottky barrier modulation is the main detection mechanism for NO₂. [3] The device responds only after the NO₂ diffuses through the protective layer. [3] However, the difference in detection mechanism between devices made with a single CNT and a CNT network device composed of multiple tubes has not yet been explored. Here I will study the sensing mechanism of devices made with CNT networks. One important reason to study networks is that CNT network devices can be made
more easily and cheaply. This is because making devices with a single CNT takes large amounts of time and effort, and there is no guarantee the CNT is semiconducting in nature. CNT network devices can be created using many standard fabrication techniques that speed production. The theoretical modeling of such devices is however much more complex than a single CNT, due to the presence of CNT junctions and the role they play in electrical current transport.

The first CNT gas sensor study tested two gases: nitrogen dioxide, NO$_2$ and ammonia, NH$_3$. These gases are common noxious gases. When a CNTFET is exposed to NO$_2$ and NH$_3$, it’s conductance changes. Figure 1-15 shows the results that occur when a device is exposed to NO$_2$ and NH$_3$. [2] NO$_2$ causes an increase in the device’s conductance and shifts the curve to the right, while the presence of NH$_3$ molecules causes the conductance of the device to drop and shifts the curve to the left. [2]
Ammonia (NH₃) is a trigonal pyramidal molecule which acts as a proton acceptor since it is a base. NO₂ is shaped like a water molecule, but its bond angles are not equal to water’s and it is an electron acceptor.

**Figure 1-15.** Conductance vs. $V_g$ graph for a CNTFET device exposed to NO₂ and NH₃ gases

**Figure 1-16.** Two dimensional representations of NH₃ and NO₂
In figure 1-16, for NH\textsubscript{3} the left hydrogen extends out of the back of the page, the middle hydrogen extends out in front of the page, and the right hydrogen is in the plane of the page. The dotted lines in the NO\textsubscript{2} diagram represent the bond which alternates between the nitrogen and the two oxygen molecules. The mechanism of charge transfer due to molecule adsorption can be explained as follows. When a NH\textsubscript{3} molecule adsorbs onto a CNT, electron charge is transferred from the NH\textsubscript{3} to the CNT. On the other hand, NO\textsubscript{2} causes charge to transfer from the CNT to the molecule. [34] Considering a p-type CNTFET, where holes are the majority carriers, this picture predicts that NH\textsubscript{3} causes conductivity in the CNT to decrease while NO\textsubscript{2} increases the conductivity, in agreement with experimental findings. [5, 34, 35] First principle calculations agree with this picture. Other theoretical works argues that NO\textsubscript{2} tends to bind more strongly with interstitial regions between tubes rather than to the sidewalls. [34, 35]

Experiments performed by other groups on thick networks of CNTs (120nm) support physical adsorption on the networks as the leading to the majority of conductance change and that molecules preferentially interact with more than one CNT. [34, 36, 37] Experimental studies of Fourier Transform Infrared Spectroscopy (FTIR) also supported this picture and showed that NO\textsubscript{2} and NH\textsubscript{3} will adsorb onto CNT meshes and interact with multiple tubes by getting trapped in interstitial regions. [35] However, conflicting experimental work of X-ray Photon Spectroscopy (XPS) concluded that above 200ºK NO\textsubscript{2} does not adsorb onto a CNT network at all, thereby ruling out charge transfer as a mechanism for CNT network sensors at room temperature. [38] The primary mechanism for the change in conductance is still debatable.

The investigations of the detection mechanism will be the main topic of this thesis. We will use the method used in our previous work for a single tube, namely selective passivation of
different regions of the device, to determine the sensing mechanism for networks and its
dependence on density. [3]

1.2 Beyond Carbon: Molybdenum disulfide

A SWNT can be described as a single sheet of graphene rolled up in the shape of a
cylinder. Both graphene and CNTs have been studied in great detail. While graphene is a
flexible material that holds promise for nanoscale electronics due to its high carrier mobility, it
has some drawbacks that limit its use in FETs, namely the lack of an intrinsic band gap. [39-44]
However, other materials that share some of graphene’s useful characteristics have come to light.
One of those materials is Molybdenum disulfide (MoS$_2$).

MoS$_2$ is a transition-metal dichalogenide semiconductor that has many uses. It can be
integrated into electronics but it also sees widespread use as a lubricant in the automotive
industry. [8, 9] The crystal structure of MoS$_2$ is two hexagonal lattices of sulfur atoms which are
bonded to an intermediate hexagonal lattice of molybdenum atoms via covalent bonds. The
group of three atomic planes (S-Mo-S) is often referred to as a MoS$_2$ monolayer. Multiple
monolayers are held together by weak van der Waals bonds. [8, 9, 39, 41] In its bulk crystalline
form, MoS$_2$ has an indirect-band gap semiconductor with a band gap of 1.2 eV. [8, 9, 39-41, 43,
44] On the other hand, the single layers have a direct band gap of 1.8 eV. [8, 9, 39-41, 43, 44]
This direct band gap combined with high mobility, gives MoS$_2$ great promise for nanoscale
electronics and stability at high temperature. [8, 9, 39-41]

Another trait MoS$_2$ shares with graphene is the fabrication technique. Single layer
graphene can be mechanically exfoliated from large chunks of bulk graphite, with nothing more
than a substrate and adhesive transparent tape. MoS$_2$ can also be exfoliated to form single layers
in the same manner. [39-41, 43, 44] The van der Waals forces that hold the S-Mo-S monolayers together are much weaker than the covalent bonds and thus the sheets readily separate. This is the key trait which allows exfoliation to take place.

The MoS$_2$ direct band gap of roughly 1.8 eV opens up the possibility for use in optoelectronic devices. The photon energy of visible light with wavelengths below 675 nm are larger than the band gap based on $E = h\nu > 1.8$ eV. This allows photons to excite electrons from the valence band of MoS$_2$ to the conduction band paving the way to optoelectronics applications. However, for practical devices, easy production and efficiency are necessary. These properties will be another topic of this work. MoS$_2$ FETs will be tested for their mobility and optoelectronic properties through the exploration of the metals used for contact electrodes. Moreover, the viability of MoS$_2$ based NO$_2$ sensors will also be tested.
Chapter 2

Design, Fabrication, and Measurement Setup

2.1 Fabrication

My samples were fabricated in the Georgetown Nanoscience and Microtechnology Laboratory (GNμLab) in the Reiss Science Building at Georgetown University. The steps necessary to fabricate each sensor include: e-beam lithography to write the catalyst island; chemical vapor deposition (CVD) to grow the carbon nanotube films; patterning the alignment marks with e-beam lithography; imaging the CNT films using the field emission scanning electron microscope (FESEM); custom fitting and writing the electrodes with e-beam lithography; and finally, covering the device electrodes with SU-8. A flow chart of the process is included in Appendix G, which outlines the fabrication process step-by-step.

2.1.1 Device design and fabrication

Design

In the original proposal for this thesis, the device design was based on a thin film of SWNTs grown by CVD directly on a Si/SiO₂ chip. The film of SWNT covered the entire 7mm x 7mm area of the chip. The experiment expanded upon previous work done at Georgetown with single tubes to a film of CNTs. Figures 2-1 and 2-2 show the general design of the initial device. This technique was not successful as it proved difficult to avoid formation of a connection
between the film and the gate electrode. This connection between the CNT film and the gate electrode shorted the FET, rendering it useless. The shorts developed from the catalyst particles finding defects in the SiO$_2$ which created an electrical connection. For this reason, the design of the devices had to be modified.

The redesigned chip reduced the area over which the catalyst was applied which reduced the chance to make a connection to the gate. The new design resembled a comb with SWNTs in between the electrodes, as seen in figures 2-3 and 2-4.
The simplicity and ease of fabrication for this device design proved not only to work well for this experiment but also made device design useful for other projects such as solid state memory devices. [37, 38, 43-44]

**Fabrication**

**Full Wafer**

The first step in fabrication is cutting 7mm x 9mm rectangular chips from a 4” Si/SiO₂ wafer. These chips will serve as the substrate of the CNTFET. Intrinsic silicon usually has a resistivity of ≈10^5 Ω·cm, but our laboratory uses a very highly doped Si with a resistivity of 0.001 – 0.005 Ω·cm. The greatly reduced resistivity of the Si substrate makes it act more like a metal than a semiconductor, and we use it as a gate electrode in our device structure.

After cleaving, the chips are cleaned using a series of organic solvents. The chips are then placed in an ultrasonic cleaner. First, they are cleaned with trichloroethylene (TCE), then
acetone (ACE), and finally isopropyl alcohol (IPA). Each cleaning stage lasts 2 minutes. A final rinse using IPA and an immediate dry using nitrogen completes the cleaning process.

*Litho Step #1*

Spin coating of the photoresist bilayer comes next. First, a layer of MMA (8.5)$^a$ (Methylmethacrylate) photoresist is spun at 4500 rpm for 45 seconds. The time and spin speed produce a resist layer of approximately 280 nm. The sample must then be baked at 180°C on a hotplate for 2 minutes to remove solvents from the MMA layer. A second photoresist, PMMA 950 C2* (Polymethylmethacrylate), is then applied using the same parameters as the MMA. These parameters produce a resist layer of approximately 180 nm. Again, the chip is baked at 180°C for 2 minutes to remove solvents from the PMMA layer. The catalyst islands are then written using Nanometer Pattern Generation System$^b$ (NPGS) software. NPGS runs on a separate PC which communicates with and directly controls the FESEM’s electron beam during the writing process. The electron beam is set to an accelerating voltage of 30 kV and the exposure dose for the PMMA/MMA bilayer is ~250-300 μC/cm². The beam exposes a comb-like pattern, figure 2-5g.

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$^a$ MMA, PMMA, and MIBK are products of Micro Chem. Corporation

$^b$ www.jcnabity.com
The small breaks between each vertical and horizontal lines were designed to improve the liftoff of the catalyst. In every chip, this pattern is written 15 times in total for a 3 x 5 array. The row to row spacing is 0.7 mm and the column to column spacing is 0.9 mm.

The chips are then developed in 3:1 IPA:MIBK* (Methyl isobutyl ketone) for 70 seconds, rinsed with IPA, and dried with nitrogen. Both MMA and PMMA are positive photoresists which means the exposed area will be washed away during development. However, MMA has a lower molecular density than PMMA so it develops faster and leaves an undercut. This structure is advantageous for the next process as well as for the metal patterning procedure.

* IPA and MIBK are organic solvents commonly used in the semiconductor industry.
used later during the fabrication sequence. The undercut caused by MMA eases the liftoff of the catalyst as well as the pattern of metal electrodes. After development, visual inspection with an optical microscope is used to ensure quality of the islands.

A pipette is then used to apply catalyst onto the chips. The catalyst solution is made by combining 114.0 mg Fe(NO$_3$)$_3$, 12.0 mg MoO$_2$(acac)$_2$, and 69.20 mg Al$_2$O$_3$ alumina (Degussa, aluminum oxide C) nanoparticles with 8ml of methanol. This recipe is derived from Lamura et al. for CNT films. [48] I have increased the amount of active components Fe(NO$_3$)$_3$ and MoO$_2$(acac)$_2$ while leaving the alumina and methanol constant, which increases the number of SWNTs grown. The catalyst particles’ sizes are the key to growing SWNTs instead of MWNTs. The size of the catalyst particles determines the diameter of the SWNTs so small particles are very important. [48] The alumina provides a structure for the islands and allows them to be optically visible, which aides the inspection of further e-beam lithography steps. An optical microscope is used to confirm that the electrode patterns are well aligned atop the catalyst islands. The solution is sonicated for 24 hours to ensure homogeneity. The catalyst solution is then diluted and sonicated for an additional 10 minutes prior to use.

The catalyst is deposited by first applying a few drops of solution onto the chip and then using the spin coater to evenly coat the sample. Each chip is spun using a three step process: a 5 second spin at 500 rpm; a 5 second spin at 2000 rpm; and a 5 second spin at 3000 rpm. Between each step, the speed is increased using a ramp rate of 250 rpm/second. This multi-stage spin process helps to ensure that an even coating is applied to the chip and helps prevent the catalyst from being thrown from the chip. The chips are then baked at 85°C for 2 minutes to evaporate
the remaining methanol thus drying the catalyst. To liftoff the photoresist, the chips are soaked in acetone. This process leaves only the catalyst islands behind. Another inspection with an optical microscope is required to ensure that the photoresist between the islands has lifted off.

**CNT Growth**

CNT growth using chemical vapor deposition (CVD) is the second major step of the fabrication process. There are several methods to synthesize CNTs such as laser ablation, arc-discharge, and CVD. Laser ablation and arc-discharge are very high temperature processes (3000°C) that create CNTs by evaporation from a large carbon source. [49, 50] The results are often large bundles of MWNTs. Moreover, the carbon source size limits the amount of CNTs produced.

CVD is an optimal technique for producing large amounts of high-quality SWNTs. [1, 49-51] High-quality, in this case, means SWNTs are relatively free of defects and amorphous carbon. CVD uses a gas as a carbon source, in this case methane, rather than a solid which favors production of SWNTs. Methane gas is the most kinetically stable hydrocarbon, which limits the thermochemical or pyrolytic decomposition during the growth process and decreases the amount of amorphous carbon produced. [49, 51] Finally, CVD is a straightforward fabrication procedure which allows for easy production of CNT devices.

The chips with patterned catalyst islands are placed into a small quartz tube known as “the boat” and pushed into the center of a furnace tube. The catalyst islands should remain facing up and the chips should be oriented so that it takes into account that CNTs grow preferentially in the direction of the gas flow.

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\(^{c}\) Appendix A details this process
Once the boat is inside, the system is purged with methane, hydrogen, and argon gas sequentially for 5 minutes each. Gas flow is controlled with precision Omega rotameters connected to standard gas cylinders. After the purge, the hydrogen and methane are shut off and the argon continues to flow as the growth furnace’s temperature zones heat up. There are three zones and they heat up to 750 °C, 900 °C, 750 °C. While CNTs can be grown at hotter
temperatures, heating at 900 °C produces high-quality CNTs. Growth is initiated when the furnace reaches the temperature set points by introducing methane (2079 sccm) and hydrogen (~633 sccm) and closing off the argon line. Thirty minutes after the introduction of hydrogen and methane, the argon line is reopened and then both the hydrogen and methane gas flows are turned off. The furnace is then left to cool under argon flow.

**Litho Step #2**

The third fabrication step patterns the alignment marks on the chip using e-beam lithography. First, the CNT networks are imaged using the FESEM. These images are a quick assessment of overall density and allow for prioritization of chips in each batch. The best chips move further along the process chain, where e-beam lithography is performed for a second time, using MMA and PMMA. The same procedure from the first step in fabrication is followed. This procedure does not impact the CNTs. NPGS and the FESEM write the alignment mark pattern around the catalyst islands with the electron beam set to an accelerating voltage of 30 kV and the exposure dose for the PMMA/MMA bilayer at ~250-300 μC/cm². The writing is followed by development in 3:1 IPA:MIBK, IPA rinse, and nitrogen dry. Again, a visual inspection of the alignment marks is made to ensure the quality of the exposures, development and that the catalyst islands are centered in the alignment marks.

As mentioned earlier, MMA’s lower density produces an undercut during development, which is useful for producing the alignment marks with sputtering of metals. Sputtering is a thin film deposition technique where a high electric field ionizes the gas in a vacuum chamber and creates a plasma. The voltage accelerates the plasma ions toward a metal target, such as

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\[d\] Appendix B details this process  
\[c\] Appendix C details this process
chromium, gold, or palladium, and ejects metal atoms from the bulk of the target which are then deposited on the sample. This technique produces high-quality uniform films of metal.

Alignment marks typically consist of a two metal stack of chromium and gold or titanium and gold. Chromium and titanium act as an adhesion layer because gold does not adhere well to SiO$_2$. The gold is needed for visibility as titanium and chrome are difficult to see on the FESEM during subsequent writing processes. The alignment marks are key to ensure that the electrode patterns are written directly on top of the catalyst islands and SWNTs. Misalignment of the electrodes could result in a non-functioning device. After sputtering the metal, the chips are left to soak in acetone which dissolves the photoresists and lifts-off the undesirable metal.

Figure 2-7. Alignment marks shown positioned around the catalyst islands
Litho Step #3

Continuing fabrication entails full imaging of the sample with the FESEM. These images are key to creating electrodes during the next e-beam lithography process. The images are imported into NPGS where the electrode pattern is superimposed on the image. The electrode pattern is adjusted and moved to cover the catalyst islands and the ends of the SWNTs.

Once again, the spinning procedures for both MMA and PMMA are repeated. The electrode pattern files are then used by NPGS to control the electrode writing. Writing and development steps are the same as earlier. Figure 2-8 shows the fabrication flow of this process and a FESEM image of a network. Figure 2-9 shows a schematic of the electrode pattern.

**Figure 2-8.** Fabrication flow for sample. a) spin coat bilayer of photoresists, b) e-beam lithography, c) development, d) sputter metal, e) lift off photoresist and excess metal, and f) FESEM image of a SWNT network with electrodes.

*Appendix D details this process.*
At this point, the samples are ready for another metallization. The contact metal is sputtered on using the same process as the alignment marks. Acetone is used to lift off the excess metal. The devices are now ready for measurement.

The first measurements are $G$ vs. $V_G$ measurements. After these measurements, the sample needs to be tested as a gas sensor in the measurement setup. If the sample proves to be an effective sensor with low noise and a large enough on-state current ($I_{DS} > 10^9$), it can then be subjected to further fabrication steps.

Figure 2-9. Electrode pattern
**SU-8 2 Litho Step**

The experiment requires the passivation of the electrodes that contact the CNTs. This is done using SU-8 2 as the main passivation layer. The “2” in SU-8 2 denotes the thickness: 2 μm. This thickness is one of the main aspects which enables the SU-8 2 to passivate the devices from the gases. Both photolithography and e-beam lithography can be used to cross-link the SU-8 2. SU-8 2 is a negative photoresist which means, contrary to MMA and PMMA, the area on the chip exposed to the electron beam will remain after development. The SU-8 2 is a polymer that changes from a more liquid state to a more solid when exposed and developed through a process called cross-linking. The molecules in the SU-8 2 will rearrange themselves and thus cross-link.

Each lithography process starts the same way. First, a coat of PMMA is spun onto the sample at 4500 rpm for 45 seconds. The sample is baked at 180°C to remove the solvent from the PMMA. The PMMA can act as a release layer to aid liftoff of SU-8, should the exposure go poorly due to misalignment or over exposure. However, this release layer is not 100% effective. PMMA is a much thinner layer than SU-8 2 (0.2 μm vs. 2 μm). Next, a coat of SU-8 is applied. Spinning requires a two-step method where the sample is ramped to 500 rpm at a rate of 100 rpm/second to evenly distribute the photoresist, the then speed is ramped to 2000 rpm at a rate of 300 rpm/second, and held for 30 seconds to coat the sample with an even 2 μm layer.

The sample needs a pre-exposure bake to remove solvents from the SU-8 2 layer. Samples are then baked at 65°C for 4 minutes. The temperature is then ramped up slowly over 5 minutes to 95°C, and the samples bake 3 minutes at 95°C. SU-8 2 and the samples have different thermal expansion coefficients. By slowly increasing the temperature, the mismatch is minimized which prevents the SU-8 2 from separating from the sample. Ramping the
temperature at or below 5°C per minute ensures that the heat is transferred evenly through the sample and photoresist layers.

As mentioned earlier, the SU-8 2 exposure can be achieved by using photolithography or e-beam lithography.

For e-beam lithography, the main difference from the previous patterning with MMA/PMMA, is the exposure dosages. SU-8 2 needs a much smaller dose of ~1-4 μC/cm² as compared to PMMA’s 250-300 μC/cm².

For photolithography, the process requires a photomask to be brought into contact with the chip. The photomask has transparent areas where the UV light (365 nm) passes through and exposes the SU-8 2. Both versions need a post-exposure bake where the sample is heated to 65°C for 4 minute, then a slow ramp up to 95°C over 5 minutes, and then held for 1 minute at 95°C. The post exposure bake finishes the chemical reaction which cross-links and hardens the SU-8. Next, the sample is placed in SU-8 developer for 1 minute to remove unwanted SU-8, rinsed with IPA, and dried with nitrogen. Finally, an inspection with the optical microscope confirms if the SU-8 2 encapsulates the metal contacts.\(^8\) Figure 2-10 visualizes the process’ fabrication steps.

\(^8\) Appendix E and F detail these processes
Connecting the devices to the experimental setup required a modification of the technique typically used by our group. Normally, after metallization, the device’s source and drain pads are wire bonded to circuit boards that connect to the measurement setup. However, there are limitations: either the devices can be destroyed with static discharge during the bonding process, or the tool can break the SiO$_2$ and produce a gate leak. Bonding also requires the source and drain pads to be relatively clean. Moreover, due to the repeated testing before and after covering the device with SU-8 2, the wire bonds must be removed and then replaced.
Due to these complications, a new test bed was designed specifically for this experiment, which was then manufactured by Leon Der in the Physics Dept. machine shop. This test bed uses pogo pins to connect the devices to the rest of the measurement setup and remove the need for wire bonding. The pogo pins are robust, easy to use, and allow for faster throughput. The sample rests on an oxygen free copper (OFC) block covered with the same varnish but does not need to be glued down. The pogo pins are screwed down using a nut driver and the resulting pressure keeps the chip in place.

![Figure 2-11. Optical image of a pogo pin apparatus.](image-url)
2.2 Measurement Setup

Gas exposure measurements are performed at Georgetown University in a vessel of our own design. The set up consists of a bell jar, aluminum plate with two electrical feedthroughs, and a gas inlet and outlet. Figure 2-12 displays a picture and simple writing schematic.

![Figure 2-12. a) A schematic diagram of the bell jar set and b) a photograph of the Bell jar](image)

The sample is placed on the OFC block and contacted using the pogo pin fixture. The OFC block rests on an aluminum stage connected to a cartridge heater. The bell jar is placed over the sample. It allows for both vacuum and gaseous measurements to be performed. The gas inlet can be connected to compressed gas cylinders, vacuum pumps, or blanks which close the inlets and outlets. The heater is used to heat the sample after measurements. Heating the sample in vacuum allows the CNT sensors to recover their original state. The ceramic tube isolates the heater from the aluminum baseplate. The heater is controlled with a custom made controller based on an Omega CN9300 temperature controller. The heater temperature can be
controlled and recorded on the computer through a Lab View program\textsuperscript{h}. The CN9300 can also be controlled independently. The thermocouple sends temperature readings to the controller allowing the controller to adjust voltage to the heater.

Electrical feedthroughs are connected to a break out box through BNC cables. A protection box is used between the sample and the voltage source as a safety measure to lower the risk of static shock destroying the CNT films. The voltage and gate bias are supplied by a HP4140B picoammeter/DC voltage source (HP). It includes two voltage sources that can be individually ramped up and down while measuring current. The HP is controlled by a custom-made Lab View program. The program allows the user to control Source-Drain voltage ($V_{SD}$), Gate voltage ($V_{G}$), and all other parameters while measuring the Source-Drain current ($I_{SD}$). The program holds the $V_{SD}$ constant, while sweeping the $V_{G}$ to preset limits after starting at 0V. The standard $V_{G}$ sweep range is -10V to 10V. During the course of the entire measurement, the program records the time, $V_{G}$, $I_{SD}$, and calculated resistance. Below is a schematic of measurement set up, figure 2-13. There is also a circuit diagram of the protection box, figure 2-14, and a simplified circuit diagram of the pico-Ammeter, figure 2-15.

\textsuperscript{h} Lab View is a product of National Instruments.
Figure 2-13. Schematic of the measurement circuit. Everything inside the dashed line is inside the bell jar.

Figure 2-14. Protection box circuit diagram.
The following chapters comprise the results and the discussion of them for all the experiments.

**Figure 2-15** Simplified electrical schematic of the HP4140B pico-Ammeter
Chapter 3

Carbon nanotube network gas sensors

3.1 Experiments, Results, and Discussion

In the past decade, gas sensing properties of CNT field effect transistors have been widely studied. [2, 4] The sensors are very attractive for their sensitivity to several gases, extremely low detection limit (ppb range), and room temperature operation. [2, 4-7] Yet to this day, there are open questions about the underlying sensing mechanism. Two main mechanisms are: charge transfer due to the physical adsorption of gas molecules onto the CNT sidewall, and the modulation of the Schottky barrier between the CNT and metal electrode contact. Previous work, including that from our laboratory, on single-CNT devices with contacts covered by a protective layer and leaving most of the CNT surface exposed, demonstrated that Schottky barrier modulation is the main detection mechanism for gas sensing. [3, 52] Here, I extended this study to CNT networks with different CNT densities. [3]

To measure the device response to NO\textsubscript{2}, we used the bell jar set up described in chapter 2. The typical measurement starts with the chamber filled with air, followed by the flow of the NO\textsubscript{2}/N\textsubscript{2} mixture. Once NO\textsubscript{2} is introduced with a constant flow (0.85 liters/min), the concentration increases from 0 to 200 ppm following the time dependence

\[
n_c(t) = (200 \text{ ppm}) \left[ 1 - e^{-t/t_0} \right]
\]

with \( t_0 = 21 \text{ (liters)}/0.85 \text{ (liters/min)} = 24 \text{ min}. \)
After a baseline measurement was taken with the device fully exposed to the gas, we used passivation layers to cover selected parts of the device. We used a dual layer of polymethylmethacrylate (PMMA) and SU-8 for the passivation. The PMMA is a positive photoresist whose presence is required only to remove the SU-8, a much thicker negative photoresist. We used the passivation layer to create two types of devices: contact-covered and fully-covered. For the contact-covered, we only cover the contact pads and leave the CNTs exposed, shown in figure 3-1. [3]

For the fully-covered device, the dual layer of PMMA and SU-8 was applied to completely cover the device, leaving the CNT and metal contacts fully passivated, as shown in figure 3-2. [3]
As described in chapter 2, we fabricated our devices using chemical vapor deposition to grow the nanotubes followed by deposition of 100 nm of Pd to form interdigitated comb-shaped metal contacts. We examined both high density and low density CNT networks where density was evaluated by counting the number of tubes that cross from one electrode to the other (C), and determining the number of junctions (J) formed between tubes. These junctions provide multiple current paths. We define density by determining the J/C ratio. The low density networks have a lower ratio of junctions to crossing tubes, e.g. J/C < 4/1. High density networks have a large number of junctions compared to crossing tubes, e.g. J/C > 4/1.

![Figure 3-2. CNT FET fully-covered with PMMA and SU-8 for passivation](image)
Subsequently, the process of selective electrical breakdown (as described in Chapter 1) was used to remove the metallic tubes from the network. [21, 25, 53, 54] This procedure destroys metallic CNTs which cause large background currents in the FET and thus enhances the on-off ratio.

For all samples, we first characterized the CNT network response by exposing the whole device (metal electrodes and CNT junctions) to a controlled concentration of NO₂. We apply a

**Figure 3-3.** a) and b) SEM images of network devices with different densities. We use the ratio of the number of carbon nanotube junctions (J) to the number of tubes crossing the electrodes (C) to characterize the density. Higher J/C indicated higher density. c) An optical image of a passivated network.
source-drain voltage \( (V_{SD}) = 20\text{mV} \) or \( 80\text{mV} \) to the single tube and network devices respectively and then sweep the gate voltage \( (V_G) \) between \(-10\text{V}\) and \(+10\text{V}\), in increments of \(0.10\ \text{V} \). We measure the source-drain current, \( I_{DS} \), as a function of \( V_G \) curves for 10 minutes in air before starting the \( \text{NO}_2 \) flow to ensure that the conductance of the device is stable. Once the device is exposed to \( \text{NO}_2 \), we record the transfer characteristics and plot the saturated conductance as a function of time and \( \text{NO}_2 \) concentration. We selected the saturated conductance values at \( V_G = -9.8\text{V} \), close to the edge of the negative voltage range, to track the device response evolution vs. time. This particular \( V_G \) value was chosen since it is close to the highest \( V_G \) value without being susceptible to noise produced by the hysteresis loop changing directions. The same procedure was also followed for a single semiconducting CNT device.

**Figure 3-4.** Conductance vs. \( V_G \) curve of fully-exposed devices for networks with different densities in a) and b), and a single CNT in c). The source drain bias is fixes at \( 80\text{mV} \) for networks and \( 20\text{mV} \) for single tubes. Black curves in d), e), and f) are conductance vs. time curves measured at a fixed gate voltage, \( V_G = -9.8\text{V} \), for fully-exposed devices. The measurements in d), e), and f) correspond to the devices measured in a), b), and c), respectively. The red curves are plots of the \( \text{NO}_2 \) concentration as a function of time.
Similar to single CNTs tested in our previous work, ref [3], all three types of devices showed that the saturated conductance tracks the NO$_2$ concentration reasonably well, as seen in figure 3-4d,e,f.

We recover all the devices in vacuum at $10^{-5}$ torr while heating to 100ºC for 10 minutes. This process returns the transfer characteristics back to pre-exposure levels. Next, for the same devices, we passivated the metal electrodes using a bilayer of photoresists, namely a layer of 200 nm PMMA and a subsequent layer SU-8 to obtain contact-covered devices, to protect the metal while leaving the CNTs and the junctions unexposed. The bilayer facilitates easy removal of the SU-8 through a PMMA lift off process. Figure 3-3c shows an optical image of a contact-covered CNT network device. We find that in this, and in previous experimental work, it is crucial to have the passivation layer extend a few microns beyond the edge of the contacts to ensure effective and complete coverage beyond the edges non-uniformity and depletion lengths due to doping of the nanotubes. [3] Complete passivation may not occur if the protective layer extends less than a micron beyond the edge of the electrode. Therefore we extend the passivation layer at least 2 µm beyond the electrodes, as shown in figure 3-3c. [55]

We then repeat the exposure to NO$_2$ for these contact-covered devices. We find that both high and low density network devices react immediately, showing the characteristic response with a shift of the hysteresis loop and an increase of saturated conductance. (figure 3-5 a,b,d,e) However, the single tube shows no noticeable response for the first 40 minutes. [3]
For the networks, we compare the contact-covered and fully-exposed response to see whether there are any notable differences with the network densities. For a high-density network, the fully-exposed and contact-covered devices show very similar responses. (figure 3-4 a,d and 3-5 a,d) On the other hand, for the low density networks, the response of the contact-covered device is notably slower than the response of the fully-exposed device (figure 3-4 b,e and 3-5 b,e), although not as slow as the single nanotube device. (figure 3-5 c,f)
Figure 3-6. Conductance vs. time curves measured at a fixed gate voltage, $V_G = -9.8$ V, for fully exposed (black) and contact-covered (red) devices in the cases of high-density ($J/C > 4$) networks a) and c) and low-density ($J/C < 2$) networks b) and d).

Figure 3-6 shows the time dependent response for the fully exposed (black) and contact-covered (red) networks corresponding to 4 different devices. We characterized the networks in terms of their density and found that the higher the network density, the smaller the change between the contact-covered and uncovered response.

To further understand the effect of the SU-8/PMMA passivation, we investigated the response of a network fully-covered with PMMA and SU-8. In this case, both the nanotube junctions and the metal contacts are passivated. We performed this on multiple samples and a
consistent behavior was observed. The fully-covered devices showed no response for the first 40 minutes of exposure to NO$_2$. After 40 minutes, the device exhibited a reaction as the gas diffused through the SU-8 layer and reached the tubes and electrodes.

The substantial delay in the response for the SU-8 covered device allows us to distinguish the contribution to the response from the covered vs. uncovered parts in the contact-covered devices. (figure 3-7) The parts of the devices that are exposed to the gas can show their response immediately, whereas the covered parts start showing a noticeable response only after 40 minutes. In the case of the contact-covered single tube, there is no measurable response for the first 40 minutes, demonstrating that the main contribution to the response is not due to the fully exposed tube sidewalls, but due to the contact interfaces. This is in agreement with our previous results on single tubes. [3]

![Figure 3-7. a) Conductance vs. $V_G$ curve for a fully covered network b) Conductance vs. time curve measured at a fixed gate voltage, $V_G = -9.8$ V, for the covered high density network. The red curve plots the NO$_2$ concentration in the bell jar as a function of time.]

However, for the networks, the devices start responding immediately. For low density networks, the overall response is weaker than when the sample is fully exposed. Whereas for the
high density networks, the contact-covered and fully-exposed responses are almost the same. This indicated that the presence of CNT-CNT junctions plays a major role in the device response. The junctions are being affected by the gas and changing the conductance. However, for low density networks with J/C < 2/1, their contribution to the response is not sufficient to recover the overall response, which is slower due to the delayed contribution of the covered electrodes. We conclude that in this case both the metal contacts and the CNT-CNT junctions contribute to the device response. In contrast, for high density networks with J/C > 4/1, the junctions fully dominate the response and the contacts do not significantly contribute, since the electrode-covered and fully exposed devices show similar responses.

This experiments of selective device exposure show that there are two main contributions to the device response. The first is the modification of the CNT-electrode interface, consistent with our previous results. The second is the increase of conductance at the CNT-CNT junctions. Notably, both cases can be explained as the response due to changes in the Schottky barriers along the source-drain current path. At the CNT-electrode contact, the Schottky barriers change due to the shift of the metal work functions. The area of a CNT-CNT junction between two nanotubes is very small, ≈ 1 nm². [56] Yet, tunnel barriers for the majority carriers form at the junctions between two metallic or two semiconducting CNTs. [56] In addition to this tunnel barrier, the junctions in the networks between metallic and semiconducting tubes form Schottky barriers [56] Assuming the work functions of both tubes are roughly equal, the $E_F$ of the metallic tube should fall inside the band gap and the SBH will be half the band gap. [56] Unlike the Schottky barrier between the electrodes and nanotube, the depletion region is twice as large for the Schottky barrier between tubes, figure 3-8b. [56]
The metallic tube depletes carriers from both “sides” of the junction and forms what appears to be two barriers back to back, see figure 3-8b. [56] Since NO\textsubscript{2} adsorption is more likely to occur at CNT-CNT junctions, the presence of adsorbed gas will change the local doping at the junctions and the CNT-CNT Schottky barriers. [57, 58] The increase in doping level will reduce

**Figure 3-8.** Schottky junction between a metallic tube sitting on top of a semiconducting tube.
the depletion width near the junctions thereby increasing the current since it becomes easier for holes to tunnel. [57, 58]

In conclusion, we have fabricated several devices made of carbon nanotube networks to elucidate their gas sensing mechanisms. When a network has a high density of nanotube junctions, they dominate the response and the electrodes play a minor role. On the other hand, when the number of junctions diminishes, as in the case for low-density networks, the electrodes start playing a substantial role in the response and eventually become the main response mechanism for single-CNT devices, where no CNT junctions exist. This illustrates that both mechanisms are at work and the density determines which mechanism is more dominant.
Chapter 4

Molybdenum Disulfide

MoS$_2$ is a very promising 2D material for nanoelectronic devices. Its large intrinsic band gap, relative ease of fabrication, and high mobility has encouraged large amounts of research. In this chapter, the effect of contact metal as well as the results of gas sensing and optoelectronic experiments will be discussed.

4.1 Fabrication

Fabrication of MoS$_2$ devices uses many of the same steps as the CNT gas sensors. The same initial procedure of cleaving and cleaning of the substrate with organic solvents and ultrasonics, described in chapter two is followed. However, the subsequent process steps do follow a slightly different order, as described in-depth below.

Litho Step #1

The first step is the patterning of alignment marks, described in the following procedure. Spin coating of the photoresist bilayer comes after the cleaving and cleaning steps. First a layer of MMA (8.5)\textsuperscript{1} photoresist is spun at 4500 rpm for 45 seconds. The sample must be baked at 180$^\circ$C on a hotplate for 2 minutes to remove solvents from the MMA layer. The second photoresist, PMMA 950 C2* is then applied using the same parameters as the MMA. Again the chip is baked at 180$^\circ$C for 2 minutes to remove solvents from the PMMA layer. This lithography step is used to create alignment marks using the NPGS software.

\textsuperscript{1} MMA, PMMA, and MIBK are products of Micro Chem. Corporation
followed by development in 3:1 IPA:MIBK, IPA rinse, and nitrogen dry. Visual inspection of
the alignment marks is made to ensure the quality of the exposures and development. After
sputtering the metal, the chips are left to soak in acetone which dissolves the photoresists and
lifts-off the undesirable metal, leaving the alignment marks. The alignment marks are created
first for two reasons. First, there is less chance for residue to build up on the film because the
MoS$_2$ films are covered with photoresist one less time. Second, having alignment marks on the
sample gives the user visual cues where on the chip to exfoliate the MoS$_2$.

**PDMS Preparation**

Mechanically exfoliating MoS$_2$ onto a substrate is easily accomplished using scotch tape.
However, this approach left residue on the chips and did not easily produce single layer flakes.
Polydimethylsiloxane is a two part silicon based polymer. It is widely used in industrial and
laboratory settings. Making PDMS is a simple process. It consists of two liquid parts, the
polymer and the curing agent. The basic recipe for creating stable PDMS requires the mixing of
a 10:1 ratio by weight of the polymer and the curing agent respectively. The two must then be
mixed vigorously to ensure that the curing agent is evenly distributed throughout the polymer.
This mixing does create one problem; air is incorporated into the mixture, and the air bubbles
obscure the transparency of the PDMS. Moreover, PDMS needs time to cure after mixing the
two parts. The PDMS is therefore divided, into smaller containers, such as a 35 mm diameter
petri dish, and placed in a vacuum desiccator. The vacuum removes the trapped gasses and
during that time, the curing reaction takes place. Normal time period for curing is between 12
and 24 hours, depending on the overall amount of PDMS in each disc shaped container and
accuracy of the ratio’s mixture. For MoS$_2$ exfoliation, complete curing is not desirable because
when PDMS is fully cured it is inert and its surface has no tackiness, some tackiness is needed to effectively remove a few layers of MoS$_2$ from the bulk. PDMS can also be baked on a hotplate at 80°C which will further/complete the curing process.

**MoS$_2$ Mechanical Exfoliation**

The weak van der Waals forces that hold layers of MoS$_2$ in a bulk molybdenum disulfide crystal together allow it to be exfoliated into thin films similarly to graphene. There are several methods to exfoliate MoS$_2$ onto the base substrate. The first used scotch tape and was pioneered with graphene. [8, 39, 59] Here we use two PDMS discs that are pressed against each other repeatedly to thin the MoS$_2$. The Si chips that we use as substrates need to be secured so that they remain stable and stationary while exfoliation occurs. To facilitate this, a piece of double sided tape is applied to a cloth lab towel. A chip is then attached to the top of the double sided tape. Two more pieces of single sided tape are applied to the edges on top of the chip. These three strips of tape keep the substrate fixed, see figure 4-1.
Continuing fabrication entails several imaging processes. First, optical microscopy is the quickest and easiest way of evaluating flakes. Molybdenum disulfide flakes on the substrates show different colors under white light. Thick flakes, above 50 nm, have a white or silver appearance. They look like bulk flakes. As the flakes thin, their color changes from white, to blue, to purple, and finally to a transparent gray. The Leitz optical microscope also allows the user to take images with a camera. (figure 4-2)

**Figure 4-1.** Diagram of the sample secured in preparation for exfoliation

*Flake Characterization*

Continuing fabrication entails several imaging processes. First, optical microscopy is the quickest and easiest way of evaluating flakes. Molybdenum disulfide flakes on the substrates show different colors under white light. Thick flakes, above 50 nm, have a white or silver appearance. They look like bulk flakes. As the flakes thin, their color changes from white, to blue, to purple, and finally to a transparent gray. The Leitz optical microscope also allows the user to take images with a camera. (figure 4-2)
Atomic Force Microscopy (AFM) is used in conjunction with the camera images to find and measure the thickness of the flake.

**Figure 4-2.** Optical image of a MoS$_2$ flakes on SiO$_2$
A single layer of MoS$_2$ has a thickness of roughly 6.5 angstroms or 0.65 nanometers. [9, 39, 41]

For our samples we typically used flakes with thickness from 15nm to 60nm. Finally, to facilitate the next e-beam lithography process, FESEM imaging of the flakes occurs. Once again these images are needed to create electrodes using NPGS.

**Litho Step #2**

Unlike the CNT gas sensors, there is no set pattern to where a flake will be with respect to alignment marks or what shape it will take. The FESEM images of the flakes are evaluated and after the images are imported into NPGS, a set of electrodes are designed to overlay on top of the flake. The spinning procedure for both MMA and PMMA is repeated. Writing and

**Figure 4-3.** AFM micrograph of a flake with carrying thickness
development steps are the same as described earlier\(^j\). Again, the metal is sputtered onto the samples and after soaking in acetone to liftoff the unwanted metal and photoresist, the samples are then ready for measurement.

### 4.2 Measurement Setup

For the electrical characterization, the devices are placed on a stage where three probes can be attached to the electrodes. The probes are connected using BNC cables to a protection box and then to a HP4140B picoammeter/DC voltage source (HP). The probe contacting the gate electrode is connected to the HP. The protection box is a safety measure that lowers the risk of static shock destroying the device. The HP is controlled by a different custom-made LabView program than the one used for the CNT gas sensors. The program differs as it allows independent control of the \(V_{SD}\), \(V_G\), and sweep rate of both, while measuring the Source-Drain current \(I_{SD}\). The program requires the user to ramp the \(V_{SD}\) from 0V to the chosen voltage then, after setting the \(V_G\) range, the user starts the \(V_G\) sweep from 0V. The slow increase and decrease \(V_{SD}\) before and after the gate sweeps protects the sample and allows it to survive for additional measurements. During the course of the entire measurement, the program records the time, \(V_G\), \(V_{SD}\), \(I_{SD}\), and calculated resistance. Below is a schematic of measurement set up.

\(^{j}\) Appendix D details this process
The bell jar was also used to characterize the MoS$_2$ devices as gas sensors, in the same manner as with the CNT gas sensors.

### 4.3 MoS$_2$ Gas Sensors

As a logical extension of the bulk of my research, the gas sensing properties of MoS$_2$ were tested. MoS$_2$ thin films have a large surface area-volume ratio which allows for a large sensing area. Research has shown that single and multiple layer MoS$_2$ FETs react to low concentrations of NO. [42] Other studies demonstrate the selectivity of MoS$_2$. [60] When compared to CNTs, MoS$_2$ shows a higher selectivity when exposed to a number of gases. [60] As explained earlier, selectivity is one of CNT-based gas sensors main weaknesses.
We tested a multilayer MoS\(_2\) device with Pd electrodes by exposing it to NO\(_2\). One of the primary obstacles with MoS\(_2\) devices on SiO\(_2\) is the large gate voltage sweep range, 100V to -100V. This complicates tracking the saturated p-type conductance vs. time as the device spends much of the sweep in the off state.

![Graph showing G vs. V\(_G\) and G vs. Time for MoS\(_2\) transistor with Pd contacts](image)

**Figure 4-5.** G vs. V\(_G\) curve for a MoS\(_2\) transistor with Pd contacts a) and G vs. Time for the same device.

There are much fewer points measured in a similar time frame as compared to a CNT gas sensor, as seen in figure 4-5b. The hysteresis of the device also prevented a stable measurement at a single gate voltage value (V\(_G\) = -99V). When the sweep was stopped the current would drop and not remain stable. These reasons made it harder and less useful to create a normalized conductance vs. Time graph as used for CNTs. However, the device did exhibit a very strong reaction, as within 24 minutes of exposure it had almost tripled it saturated current from 2.58 nA to 6.7 nA.

Another drawback with the test device was its lack of recovery. When treated with the same recovery procedure as the CNT sensor (vacuum level of 10\(^{-5}\) torr and heating of the sample...
to 100°C for 10 minutes) the MoS$_2$ samples performance deteriorated. The on current was reduced by an order of magnitude and the signal to noise ratio decreased greatly. One possible explanation for this result was that adsorbed gas causes a degradation of the contacts when it releases. [60] However, further experiments must be performed to confirm this. Considering this factor and the difficulty in fabrication, more devices were not allocated to this experiment. More work needs to be done to assess the viability of MoS$_2$ for practical gas sensing applications.

4.4 MoS$_2$ device Mobility

One of the desirable characteristic of MoS$_2$ is its reasonably high charge mobility reported to be $\approx$200 cm$^2$/V·s in dual-gated single layer devices. [8, 9, 39-41, 61, 62] This value was higher than previously reported [59, 63] and it has been later revised by taking into account the coupling of top and bottom gate capacitance. [62] The actual mobility was then estimated to be one order of magnitude smaller. [62] Carrier mobility is proportional to current thus the higher the mobility the more current materials/devices can carry. In transistors, high mobility means that fewer electrons or holes need to move to create higher currents. This leads to better device performance. Metals such as Au, and titanium are commonly used for MoS$_2$ FETs in current literature. We fabricated devices with Au electrodes as well. However, extending from our CNT research, the use of Pd was also a logical choice. We found that the MoS$_2$ fabrication procedure created problems of adhesion with Pd, therefore for Pd samples, we used a Nb adhesion layer (1-3nm). Most devices were contacted with 2 μm wide electrodes with a 2 μm gap. The area of the MoS2 channel varied as the shapes were non-uniform.
For similar flake areas, Pd and Nb devices demonstrated larger on-currents compared to Au. Since Nb electrodes yielded the largest on currents, we tested the mobility for devices with Nb electrodes. Mobility has been shown to improve in devices passivated with a thin layer of a high-\(k\) oxide \([39, 64]\), therefore we deposited a layer of Al\(_2\)O\(_3\) on the Nb samples.

High-\(k\) dielectrics are often fabricated using a process known as Atomic Layer Deposition (ALD). ALD uses multiple precursor gasses to create atomic layers of the oxide one by one. The substrate will be exposed to the precursor gasses one at a time in a specific sequence to limit the reaction. For Al\(_2\)O\(_3\), the precursors used are Trimethylaluminum (TMA) and ozone. TMA provides the Al and ozone provides the oxygen to the oxide. Water can be substituted for ozone as a source of oxygen in ALD processes. When done correctly, high quality oxides are created. These oxides can also be deposited on patterned substrates for top gates or for passivation layers for gas sensors. Care must be taken due to the temperatures required in ALD, since PMMA can fully cross-link and become hard above 200\(^\circ\)C, preventing liftoff of PMMA and the extra oxide.

Calculating carrier mobility is relatively simple: it was calculated using the formula,

\[
g_m = \mu_n \, C_{OX} \left(\frac{W}{L}\right) V_{SD}
\]

where \(g_m\) is the transconductance, \(\mu_n\) is the mobility, \(C_{OX}\) is the capacitance of the oxide, \(W\) and \(L\) are the width and length of the MoS\(_2\) channel, and \(V_{SD}\) is the source-drain voltage. The transconductance is defined as \(g_m = \frac{dI_{DS}}{dV_{GS}}\). The flakes dimensions were 2 \(\mu\)m by 2 \(\mu\)m and the \(C_{OX}\) was calculated to be 1.2X10\(^{-4}\) F\(\cdot\)m\(^2\). The hole mobility for this device is 4.05 cm\(^2\)/V\(\cdot\)s.
The device was then covered with a 15 nm layer of Al$_2$O$_3$ and the transfer curve was re-measured. The current did saturate but at a lower current level and the hysteresis increased compared to the curves of the device before coverage, shown in figure 4-6.

![Figure 4-6. MoS$_2$ transistor with Nb contacts before and after Al$_2$O$_3$ passivation](image)

The device also turned on at a lower $V_G$ value. Unfortunately, the calculated mobility did not improve as hoped. The $\mu_0$ was measured to be 1.27 cm$^2$/V•s, a drop of roughly 75%.

One simple explanation for the decrease in mobility and the increase in hysteresis is the quality of the oxide. A MMA and PMMA bilayer was patterned so the oxide could be deposited
to cover only the device area. However, in the patterning process, the current in the SEM was fluctuating, leaving some cross-linked specks of MMA/PMMA, as seen in figure 4-7.

None were directly on top of the MoS$_2$ but this hurt the oxide quality possibly creating traps for charges when sweeping the gate voltages. Moreover, the oxide was deposited at 150°C which is low compared to other processes. This lower temperature was needed to protect the photoresist and the device itself. More trials are needed to better investigate the mobility and ways to improve it. One of the most important factors is better control of the Al$_2$O$_3$ deposition and quality. While ALD can produce good quality oxide, the process must be experimented with further to reliably produce a good layer even in the presence of photoresists.

Figure 4-7. Optical image of a MoS$_2$ transistor passivated with Al$_2$O$_3$
4.5 Photovoltaic MoS$_2$ Devices

Due to its energy band gap, MoS$_2$ can be integrated into field effect transistors. One of the challenges associated with MoS$_2$ devices was the lack of the $p$-type conductance. All previous research, on solid state devices showed device with $n$-type conductance. [8, 9, 39-44] The only way to see any $p$-type conduction was through ionic liquid gating or the use of PMMA as an additional dielectric layer under the MoS$_2$. [65, 66] While these techniques demonstrated a proof of concept, they added an additional layer of challenges for integration into full-scale production devices. Our samples made with Pd electrodes and standard fabrication techniques were there first $p$-type fully solid-state devices. [67]

This difference in polarity for our devices was determined by the choice of electrode material. When Pd is sputtered as the source and drain electrodes with a thin Nb layer as an adhesion layer, the MoS$_2$ transistors always show $p$-type behavior. When we use Cr as the adhesion layer and Au as the main contact, the devices show the typical $n$-type behavior obtained by other groups. The adhesion layers of Cr and Nb, for the Au and Pd contacts respectively, are extremely thin, sub 3 nm, and do not form a continuous film. Therefore, the majority contact area between the flake and electrodes will be formed by the MoS$_2$/Pd and MoS$_2$/Au interfaces. Furthermore, devices fabricated with only Nb electrodes show $n$-type behavior (see figure 4-8), affirming that the $p$-type behavior in Nb/Pd devices is solely due to the MoS$_2$ interface.
Figure 4-8. Transfer characteristics of MoS$_2$ transistors. **a**, MoS$_2$ transistor with Au contacts. Only $n$-type behavior is observed. **b**, MoS$_2$ transistor with Pd contacts. Only $p$-type behavior is observed. **c**, MoS$_2$ transistor with Nb contacts. Only $n$-type behavior is observed.

Figure from [67]

We therefore decided to fabricate devices made with two different contact materials, Au for one electrode and Pd for the other, demonstrate asymmetric ambipolar behavior. These
devices also displayed diode characteristics for a wide range of gate voltage. A logical explanation of these results is to assume different work functions for Pd, MoS$_2$, and Au. The literature gives a range of values for the work function of MoS$_2$, $\Phi_{\text{MoS}_2}$, from 4.48 eV to 5.2 eV. [68-70] We used a Kelvin probe system to measure the work function of our Au and Pd films and found that they are very close, $\approx$5.1 eV, in agreement with values reported in the literature. [68-70] Examining these values alone will not explain the difference in device behavior, thus different interactions at the interface between the MoS$_2$ and Pd and the MoS$_2$ and the Au may be the cause of a shift $\Delta \Phi$ in the band alignment. [67]

Assuming that the Fermi levels of three material satisfy $E_{\text{F, Pd}} < E_{\text{F, MoS}_2} < E_{\text{F, Au}}$, as seen in figure 4-9a and b, the charge transfer that occurs at each interface will yield Schottky barriers either upward (hole doping) or downward (electron doping) bending of the conduction and valence band edges.
Figure 4-9. Schematic band alignment for different source and drain electrode materials. **a**, Two Au electrodes. **b**, Two Pd electrodes. **c**, One Au and one Pd electrode. In **a**, **b**, and **c**, the left panel shows band alignment before contact and the right panel illustrates the band bending after contact. The shift in bands upon application of a gate voltage is also shown. **d**, Effect of source-drain bias on device with one Au and one Pd electrode. Figure from [67]
This band alignment can justify both the polarity of the MoS$_2$ FETs made with Pd or Au as source and drain electrodes and the diode characteristic we obtained for MoS$_2$ flakes made with Pd and Au as two different materials for source and drain electrodes. (figure 4-9a,b,c,d) [67]

We tested the photoresponse of diodes with Pd-Au electrodes and measured a clear photovoltaic effect. [67] From the open-circuit voltage and the short circuit current, we can estimate the maximum electrical power that can be removed from the device, about 2.5% of the incident laser power between the electrodes. Since only the depletion region in the MoS$_2$ channel is photoactive, this percentage is just a lower bound for the conversion efficiency. Nevertheless, this room-temperature efficiency is better than the highest value previously reported in MoS$_2$, about 1% at 120K for bulk samples. [71]

Figure 4-10. Photovoltaic effect with Pd-Au bias configuration. a, Optical image of the device. The spacing between the electrodes is 2 μm. b Current vs. source-drain voltage at $V_G$ = 0 showing strong asymmetry and photoresponse with diode-like behavior for Pd-Au bias configuration indicated in a Figure from [67]

We conclude that multilayer MoS$_2$ solid-state transistors can be polarity controlled by choosing appropriate electrode materials. Au and Pd despite their similar work functions produce very different device behavior. The discovery of a simple method of making $p$-type
MoS$_2$ FETs and the ability of control the polarity opens up new possibilities for MoS$_2$. Although we demonstrate photovoltaic effect, further work is needed to improve the efficiency of the device possibly by using arrays of FETs, optimizing spacing, and studying dependence on layer thickness.
Appendix A:

**e-beam lithography process for catalyst islands patterning**

1. Cut 7mm X 10 mm rectangles from doped Si/SiO\(_2\) wafer.

2. Clean chips using an ultrasonic cleaner in TCE (Trichloroethylene), ACE (Acetone), and IPA (Isopropyl alcohol) for 2 minutes in each solvent. Rinse with IPA and immediately dry with nitrogen.

3. Spin MMA (8.5)\(^k\) photoresist at 4500 rpm for 45 seconds.

4. Bake at 180°C on a hotplate for 2 minutes.

5. Spin PMMA 950 C2\(^*\) (Polymethylmethacrylate) at 4500 rpm for 45 seconds.

6. Bake at 180°C on a hotplate for 2 minutes.

7. Use Nanometer Pattern Generation System\(^l\) (NPGS) to control the FESEM’s electron beam to write catalyst islands. The electron beam is set to an accelerating voltage of 30 kV and the exposure dose for the PMMA/MMA bilayer is \(\sim 250-300 \mu\text{C/cm}^2\).

8. Develop in 3:1 IPA:MIBK\(^*\) (Methyl isobutyl ketone) for 70 seconds, rinse with IPA, and blow dry with nitrogen.

9. Use a pipette to apply catalyst onto chips. The catalyst solution was fabricated. With 114 mg Fe(NO\(_3\))\(_3\), 12.0 mg MoO\(_2\) (acac)\(_2\) and 69.20 mg Al\(_2\)O\(_3\) alumina (Degussa, aluminum oxide C) nanoparticles in 8 ml methanol. It is sonicated for 24 hours to ensure homogeneity and then it is diluted before spun onto chips. The diluted catalyst is also sonicated prior to use.

\(^k\) MMA, PMMA, and MIBK are products of Micro Chem Corporation

\(^l\) www.jcnability.com
10. Spin the catalyst first ramping to 500 rpm for 5 seconds at 250 rpm/second, then ramping up at 2000 rpm for 5 seconds, and then ramp to 3000 rpm for 5 seconds.

11. Bake at 85°C for 2 minutes.

12. Soak in Acetone to liftoff photoresist and leave catalyst islands.

13. Inspect with the Lietz optical Microscope

![Catalyst island pattern](image)

**Figure A-1.** Catalyst island pattern
Appendix B:

**CVD synthesis of carbon nanotubes**

1. Place chips with patterned catalyst islands in small quartz tube known as the boat. Have catalyst island facing up and 10mm side perpendicular to length of boat.

2. Purge methane, hydrogen, and argon gas lines for ~5 minutes each. Close hydrogen and methane but leave the argon flowing.

3. Turn on carbon nanotube furnace and set the three temperature zones. From left to right, the three zones are set to 750 °C, 900 °C, 750 °C. Fig X shows the furnace and boat. It will take the furnace roughly 1 hour to heat up to set points.

4. Start growth when the furnace reaches the temperature set points by introducing methane (~2000 sccm) and hydrogen (~600 sccm) and close off argon line.

5. After 30 minutes, open the argon line and then turn off both the hydrogen and methane. Set the three temperature zones to 20 °C and let the furnace cool with the argon flowing.
Figure A-2. Carbon nanotube furnace
Appendix C:

**e-beam lithography process for alignment mark patterning**

1. Spin MMA (8.5)\(^m\) photoresist at 4500 rpm for 45 seconds.

2. Bake at 180°C on a hotplate for 2 minutes.

3. Spin PMMA 950 C2* (Polymethylmethacrylate) at 4500 rpm for 45 seconds.

4. Bake at 180°C on a hotplate for 2 minutes.

5. Use Nanometer Pattern Generation System\(^n\) (NPGS) to control the FESEM’s electron beam to write catalyst islands. The electron beam is set to an accelerating voltage of 30 kV and the exposure dose for the PMMA/MMA bilayer is ~250-300 μC/cm\(^2\).

6. Develop in 3:1 IPA:MIBK* (Methyl isobutyl ketone) for 70 seconds, rinse with IPA and blow dry with nitrogen.

7. Inspect with the Lietz optical Microscope.

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\(^m\) MMA, PMMA, and MIBK are products of Micro Chem Corporation

\(^n\) www.jcnabity.com
Figure A-3. Alignment Marks with respect to catalyst islands

Figure A-4. Array of catalyst islands and alignment marks as it appears on samples
Appendix D:

**e-beam lithography process for electrode patterning**

1. Image samples using FESEM.

2. Spin MMA (8.5)° photoresist at 4500 rpm for 45 seconds.

3. Bake at 180°C on a hotplate for 2 minutes.

4. Spin PMMA 950 C2* (Polymethylmethacrylate) at 4500 rpm for 45 seconds.

5. Bake at 180°C on a hotplate for 2 minutes.

6. Load an image of a network into Nanometer Pattern Generation System\(^p\) (NPGS) and design the electrode pattern.

7. Use (NPGS) to control the FESEM’s electron beam to write electrodes. The electron beam is set to an accelerating voltage of 30 kV and the exposure dose for the PMMA/MMA bilayer is ~250-300 μC/cm\(^2\).

8. Develop in 3:1 IPA:MIBK* (Methyl isobutyl ketone) for 70 seconds, rinse with IPA and blow dry with nitrogen.

9. Inspect with the Lietz optical Microscope

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\(^o\) MMA, PMMA, and MIBK are products of Micro Chem Corporation

\(^p\) www.jcnabity.com
Figure A-5. Electrode pattern
Appendix E:

**e-beam lithography process for electrode masking**

1. Spin PMMA 950 C2\(^{9}\) (Polymethylmethacrylate) at 4500 rpm for 45 seconds.

2. Bake at 180°C on a hotplate for 2 minutes.

3. Spin SU-8* 2 in 2 step method: ramp to 500 rpm at a rate of 100 rpm/second then ramp to 2500 rpm at a rate of 300 rpm/second and hold there for 30 seconds.

4. Bake samples at 60°C on a hotplate for 1 minute, then slowly ramp the temperature to 90°C and hold there for 3 minutes.

5. Load an image of a network into Nanometer Pattern Generation System\(^{\dagger}\) (NPGS) and design the electrode masking pattern.

6. Use NPGS to control the FESEM’s electron beam to write catalyst islands. The electron beam is set to an accelerating voltage of 30 kV and the exposure dose for the SU8-2 ~1-4 μC/cm\(^2\).

7. Bake samples at 60°C on a hotplate for 1 minute, then slowly ramp the temperature to 90°C and hold there for 1 minute.

8. Develop in SU-8 developer for 60 seconds, rinse with IPA and blow dry with nitrogen.

9. Inspect with the Lietz optical Microscope.

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\(^{9}\) MMA, PMMA, and MIBK are products of Micro Chem Corporation

\(^{\dagger}\) www.jcnabity.com
Appendix F:

**Photolithography process for electrode masking**

1. Spin PMMA 950 C2\(^a\) (Polymethylmethacrylate) at 4500 rpm for 45 seconds.

2. Bake at 180\(^\circ\)C on a hotplate for 2 minutes.

3. Spin SU-8\(^*\) 2 in 2 step method: ramp to 500 rpm at a rate of 100 rpm/second then ramp to 3000 rpm at a rate of 300 rpm/second and hold there for 30 seconds.

4. Bake samples at 60\(^\circ\)C on a hotplate for 1 minute, then slowly ramp the temperature to 90\(^\circ\)C and hold there for 3 minutes.

5. Expose the sample under UV light for 3 seconds with a photomask. The pattern of the photomask is shown in figure.

6. Bake samples at 60\(^\circ\)C on a hotplate for 1 minute, then slowly ramp the temperature to 90\(^\circ\)C and hold there for 1 minute.

7. Develop in SU-8\(^*\) developer for 60 seconds, rinse with IPA and blow dry with nitrogen.

8. Inspect with the Lietz optical Microscope.

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\(^a\) PMMA, SU-8 2, and SU-8 developer are products of Micro Chem Corporation
Appendix G:

Fabrication Flow Chart

1. **Full wafer**
   - Cut wafer into chips
   - Clean chips

2. **1st Litho Step**
   - Spin photoresists
   - E-beam expose/develop catalyst islands
   - Spin coat catalyst
   - CNT Growth

3. **2nd Litho Step**
   - Image samples
   - Spin photoresists
   - E-beam expose/develop alignment marks
   - Sputter Metal for marks

4. **3rd Litho Step**
   - Image samples
   - Spin photoresists
   - E-beam expose/develop electrodes
   - Sputter Metal for electrodes
   - Test Samples

5. **SU-8 Litho Step**
   - Image samples
   - Spin photoresists
   - Exposure/develop electrode covering
   - Retest Samples
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